Characterization of the TriP Chip Running at 132 nsec Using a Modified AFE Board.

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1 Introduction

In this note we describe the first set of tests done with a sample of TriP chips that were mounted on a modified AFE board. The modifications consisted of different firmware and the replacement of one power supply switch. The board used was a standard AFE-Ic board (red type) on which new MCMs (MCMIIs) were mounted. The new MCMs were designed to support the TriP and emulate the SVX for readout when mounted on an AFE-Ic board. The TriP and the MCMs are described in more detail in Ref. [1].

Two versions of the MCMII were designed and built: one (MCMIIb) supports two TriP chips wire-bonded directly to the MCM substrate. The other, (MCMIIc) supports one TriP which can be either wire-bonded directly or packaged into a standard TQFP surface mount package. Due to space constraints, this MCM can support only 1 TriP. Also mounted on each MCM are all the electronics which are needed for the TriP but not present on the AFE board. This includes two dual input ADCs (AD9201), a Xilinx Field Programmable Gate Array (FPGA) (XC2S30-144) type, 2 separate LDO 2.5V linear regulators (REG113 type) to provide analog (VDDA) and digital (VDDD) supply voltages for the TriP, another dual LDO regulator (TPS74HD325) to provide power for the core and IO of the FPGA and the associated capacitors and resistors.

So far, we have tested 6 TriP chips on 3 different MCMIIb (MCMIIb-1, MCMIIb-2 and MCMIIb-3) and 2 other TriPs were tested on MCMIIc, one of them with an unpackaged TriP (MCMIIc-1) and the other with a packaged TriP (MCMIIc-2).

A set of 10 programmable internal registers control aspects of the TriP operation, the description of these registers can be found elsewhere [1]. Table 1 shows the list of the values used for the tests described in this note.

Table 1: Table of registers values for the operation of the trip. (1): does not correspond to the default value for the register. (2): the discriminator threshold is set to VTH=210 unless otherwise noted.

Name	Register address	Register value
IBP	1	130 (1)
IBBNFol1	2	120
IFF	3	20 (1)
IBPIFF1REF	4	160
IBPOMAMP	5	138
IBPFol2	6	24
IFFP2	7	42
IBCOMP	8	10 (1)
VREF	9	150 (1)
VTH	10	210 (1) (2)

In Ref. [1] there is a description of the signals that are needed to operate the TriP chip. We generate these signals using the FPGA mounted on each MCM. We implemented this with a set of shift registers that allow us to download (via the 1553 interface to the AFE board), any desired timing for the signals that the FPGA has to send to the TriP chip. These registers are run with a 121.21 MHz clock (which is 16x the crossing clock and phase locked to it), which means that each bit corresponds to a time interval of 8.25 nsec. Finer control of timing is possible, but this changing the programing of the FPGA and recompiling. The bits downloaded to these shift registers inside the TriP are listed in Table 2.

Table 2: Timing diagram for the operation of the TriP. Two different option for DIGEN were tested for this report. They correspond to options (A) and (B) in this table. Other signals were set as shown.

description	byte0	byte1
DIGENUP	00000000	00000010
DIGRSTB	01111111	11111111
PRE2BRSTB	00000011	11111100
PRERST	01111000	00011110
DIGEN(Option A)	11111111	11111111
DIGEN(Option B)	00000000	00000111

2   Discriminator Scan

As a first step in getting an understanding of the performance of the TriP we performed charge injection scan on each of the chips. The scans were done with the registers described in Table 1 and the timing specified in Option (A) of Table 2. Charge was injected on one channel at a time using the programmable charge injection mechanism in the Trip. For each value of the input change, the occupancy of the discriminators was averaged over 200 events and the results are shown in Figs. 1, 2, 3, 4, 5 and 6. Because the TriP chip has 32 channels separated in two banks of 16 channels and we want to understand possible difference between the two banks, the discriminator occupancy curves are plotted independently for each bank.

There is no scan for MCMIIb-3-Trip1, because that chip could not be turned on. It was determined that the chips has a short in the VDDA (analog power) net. This is a fabrication failure and should be considered when we estimate the yield for the TriP fabrication process. If we include the two chips tested on the bench by A.M. (the chip designer), the yield is 9/10.

In order to measure the active time window of the TriP chip when it is operated according to Option (A) in Table 2, we varied the delay of the charge injection pulse and recorded the discriminator occupancies. This was done injecting 20 fC charge in one channel at a time, and 200 events were recorded for each step. The results of this delay scan for MCMIIc-1 are shown in Fig. 7.
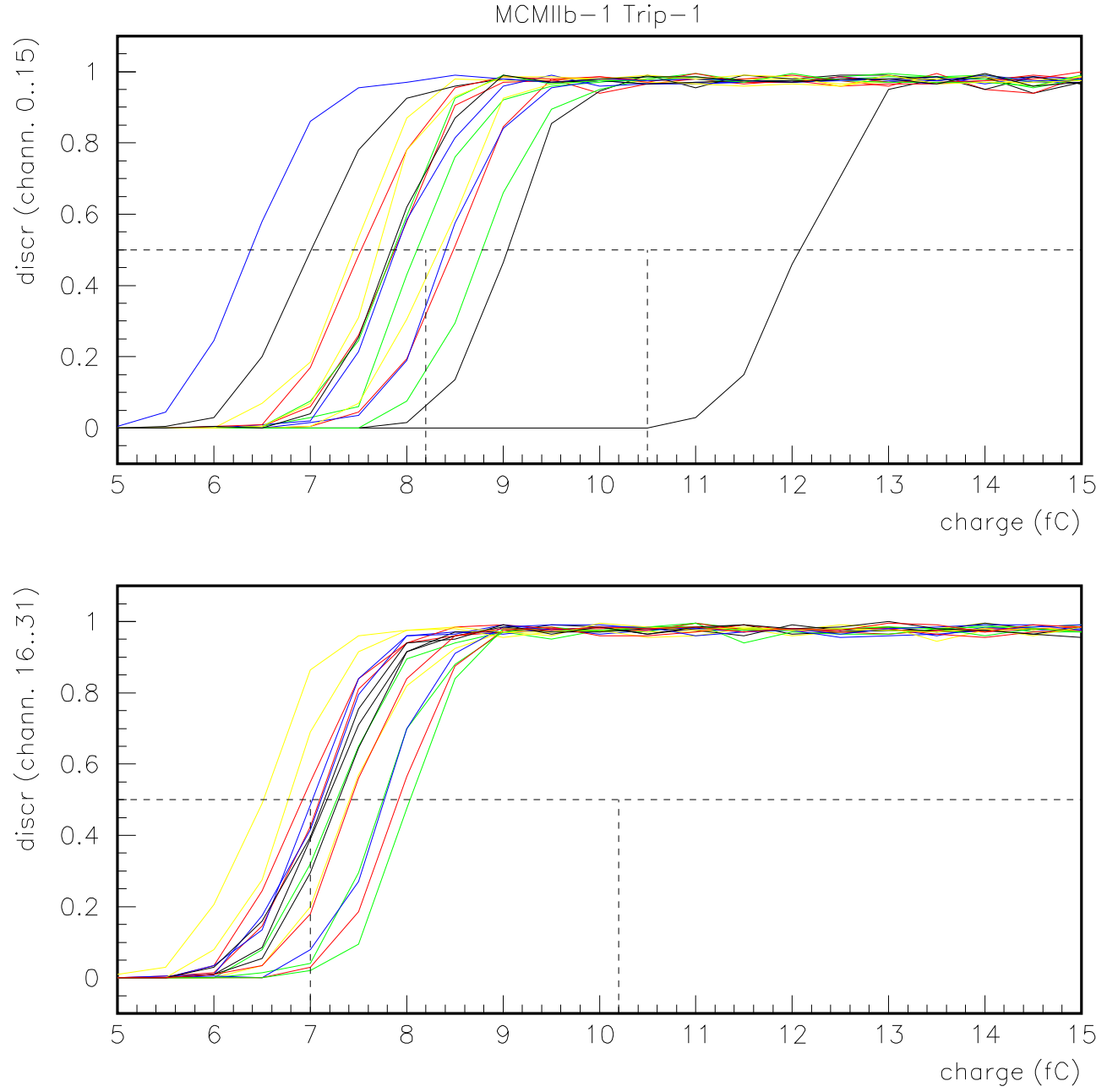
MCMIIb−1 Trip−1

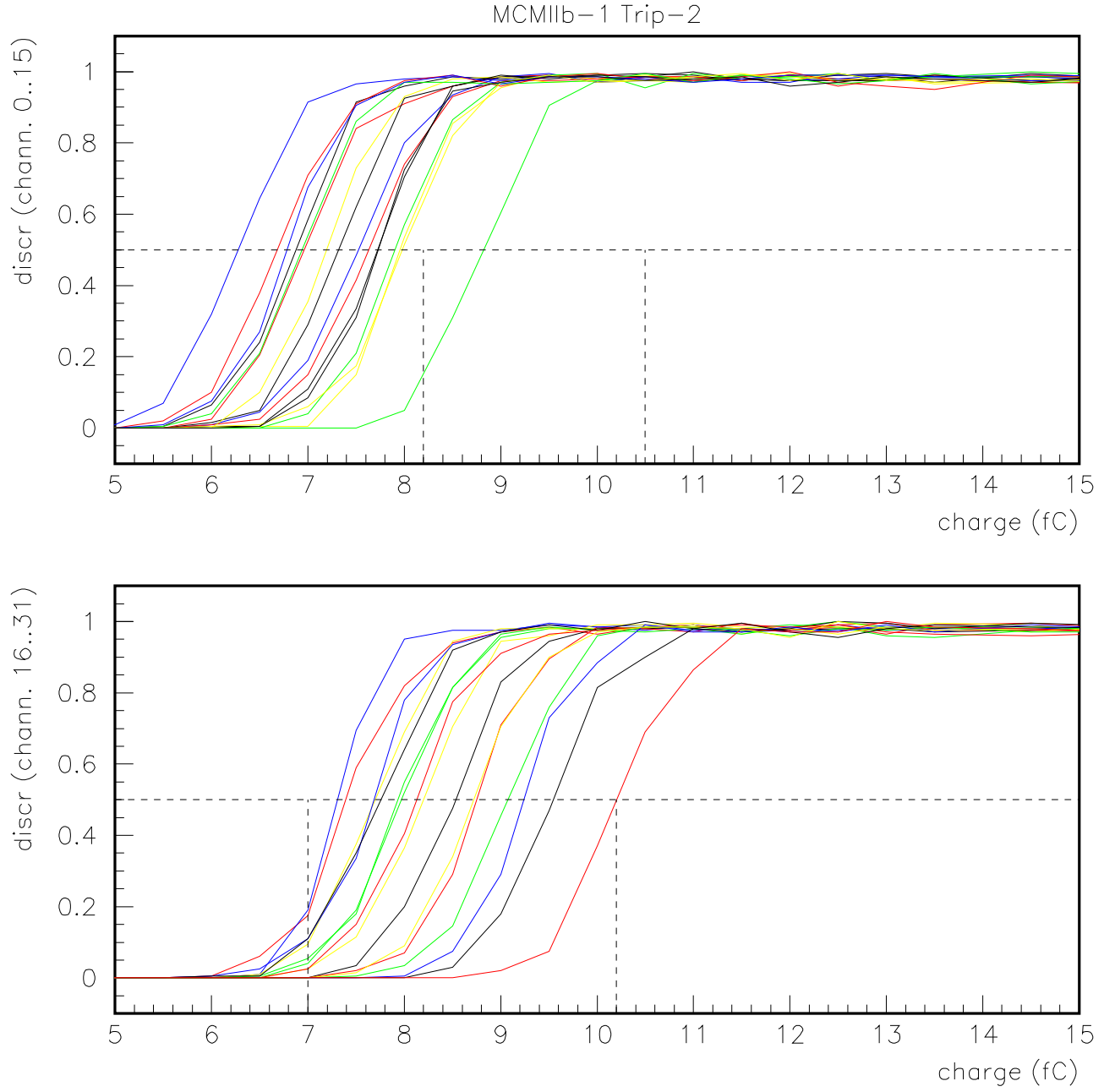Figure 1: Discriminator scan for MCMIIb-1-Trip1.

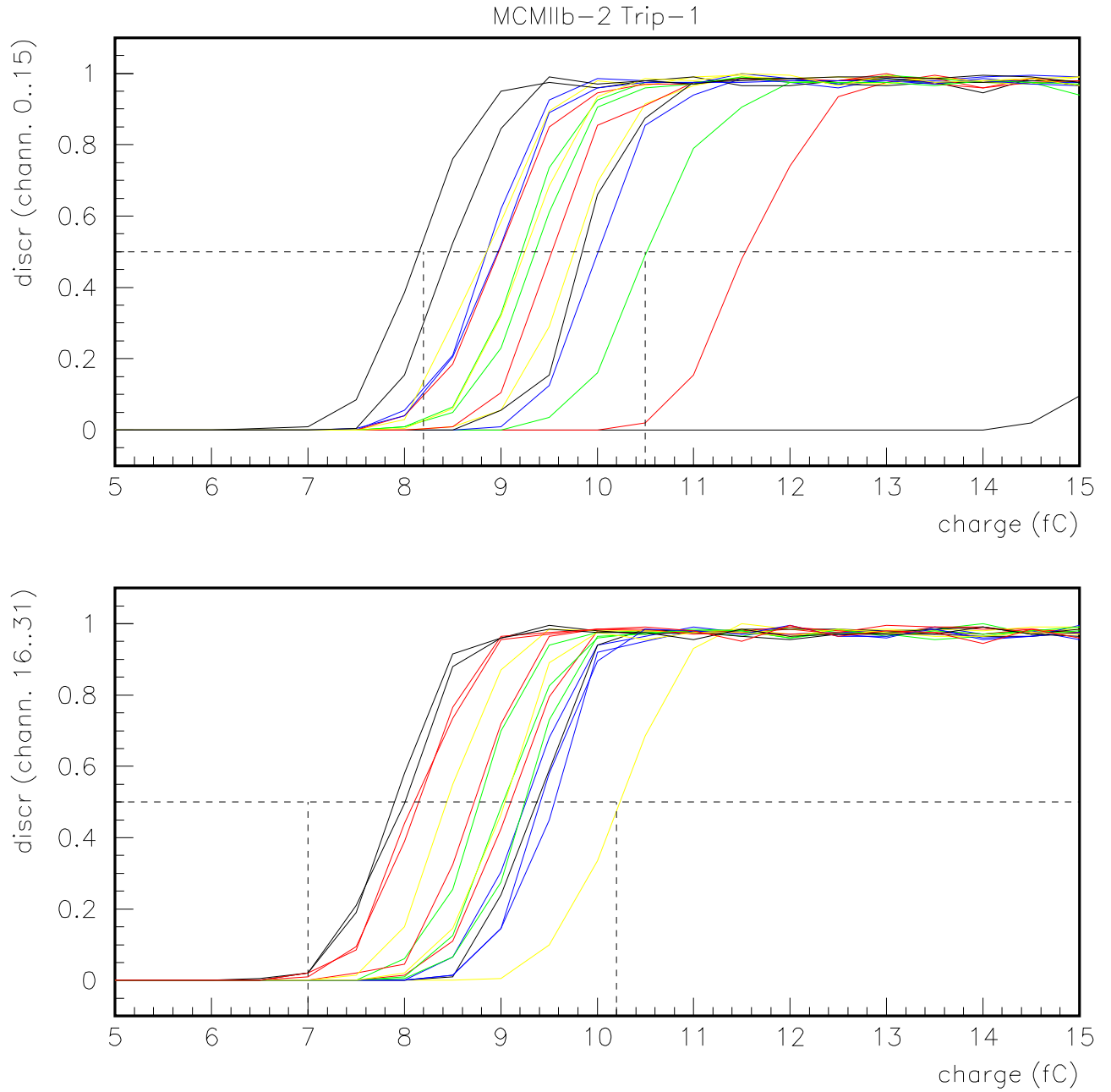Figure 2: Discriminator scan for MCMIIb-1-Trip2.
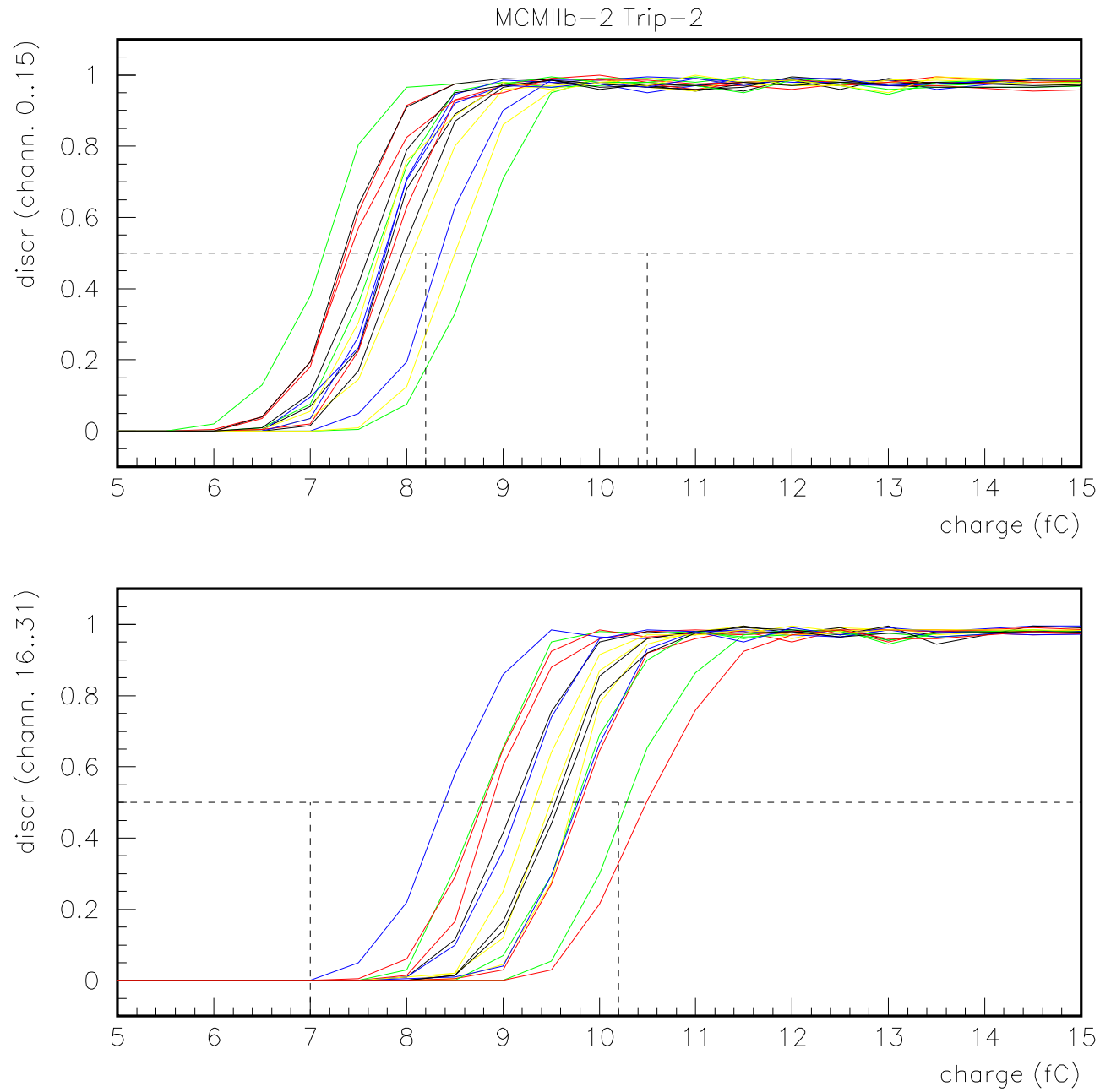
Figure 3: Discriminator scan for MCMIIb-2-Trip1.

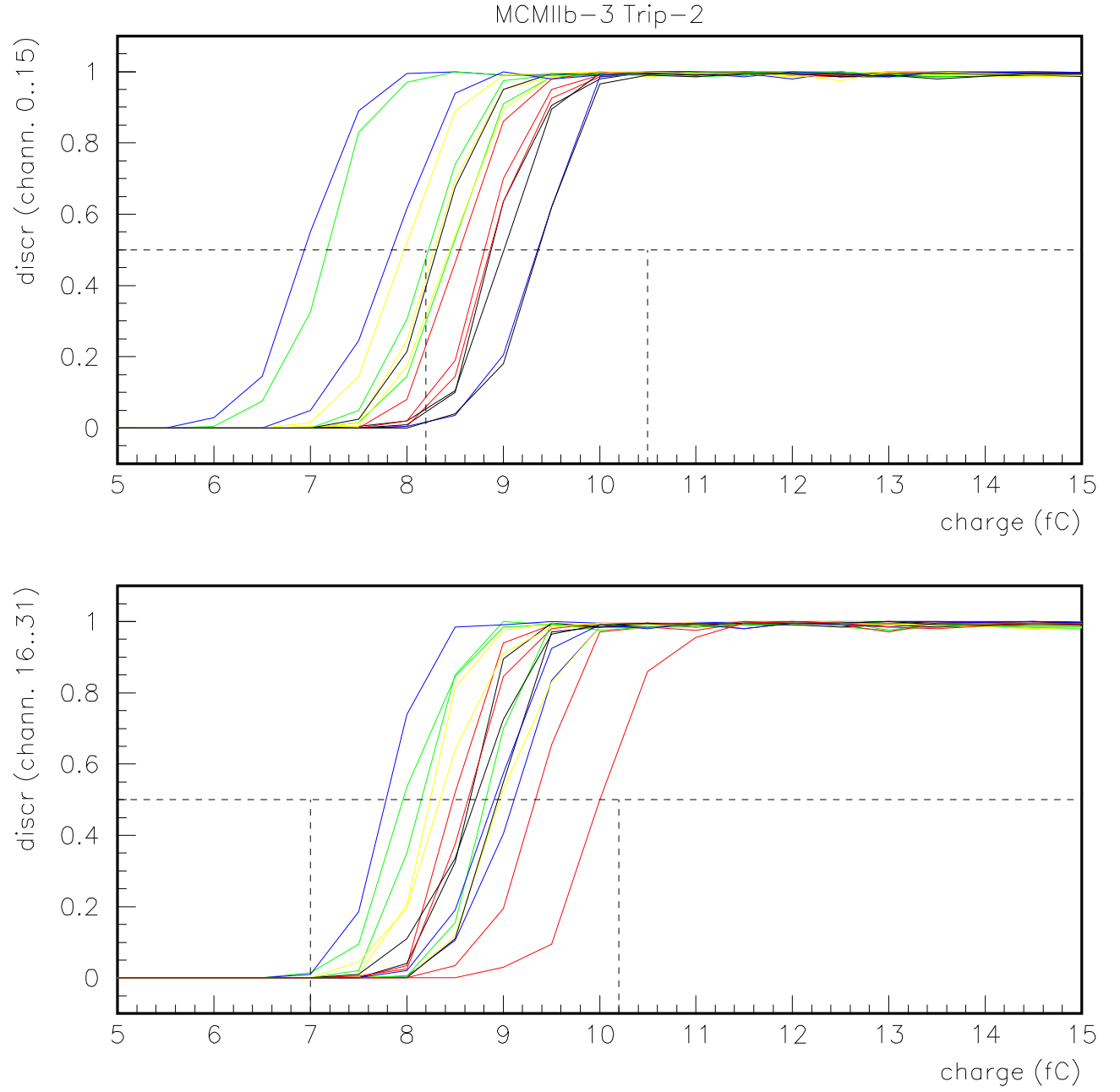Figure 4: Discriminator scan for MCMIIb-2-Trip2.

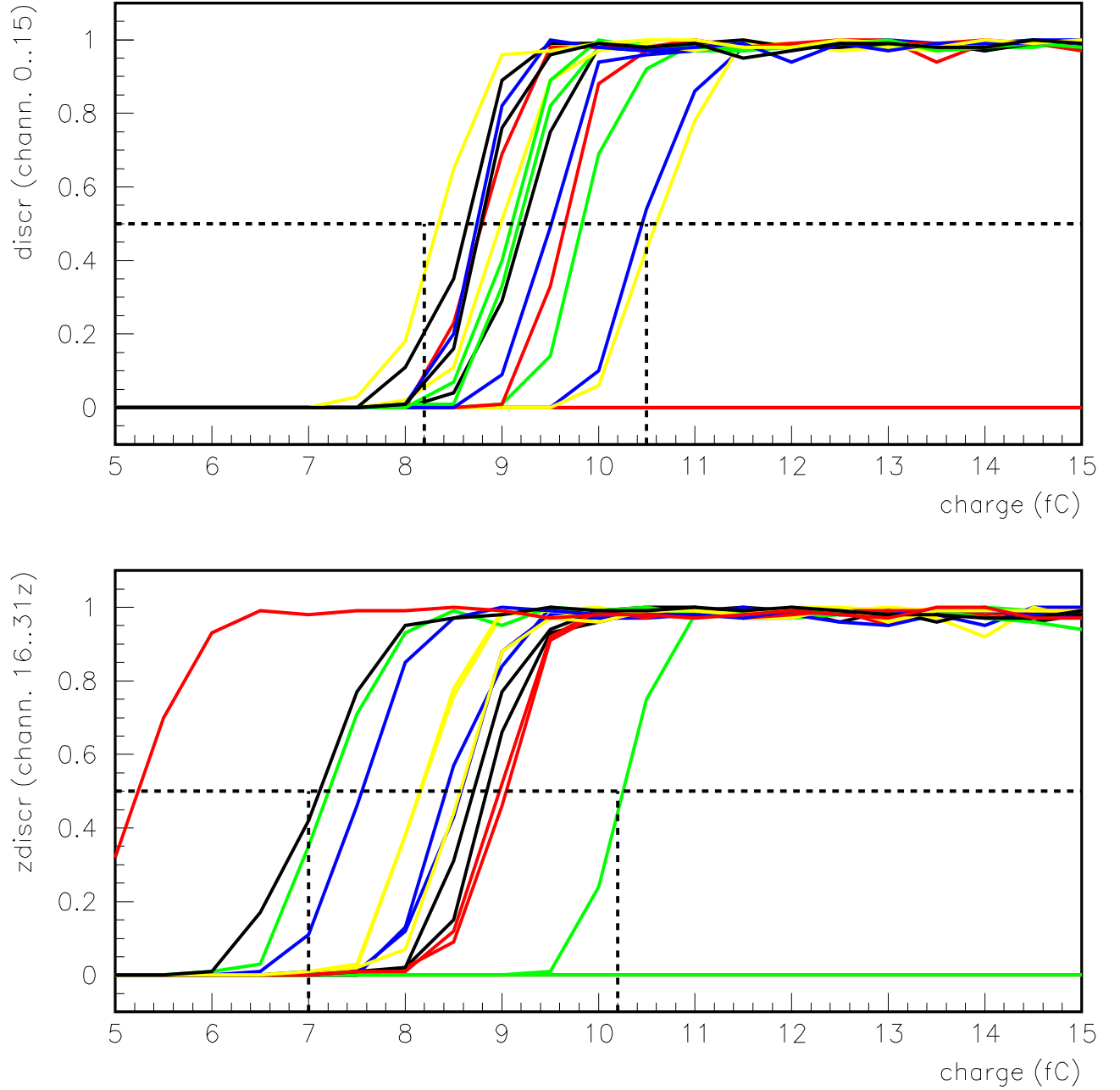Figure 5: Discriminator scan for MCMIIb-3-Trip2.

Figure 6: Discriminator scan for MCMIIc-1-Trip2. (MCMIIc has only one TriP, that for layout reasons we call TriP 2.)
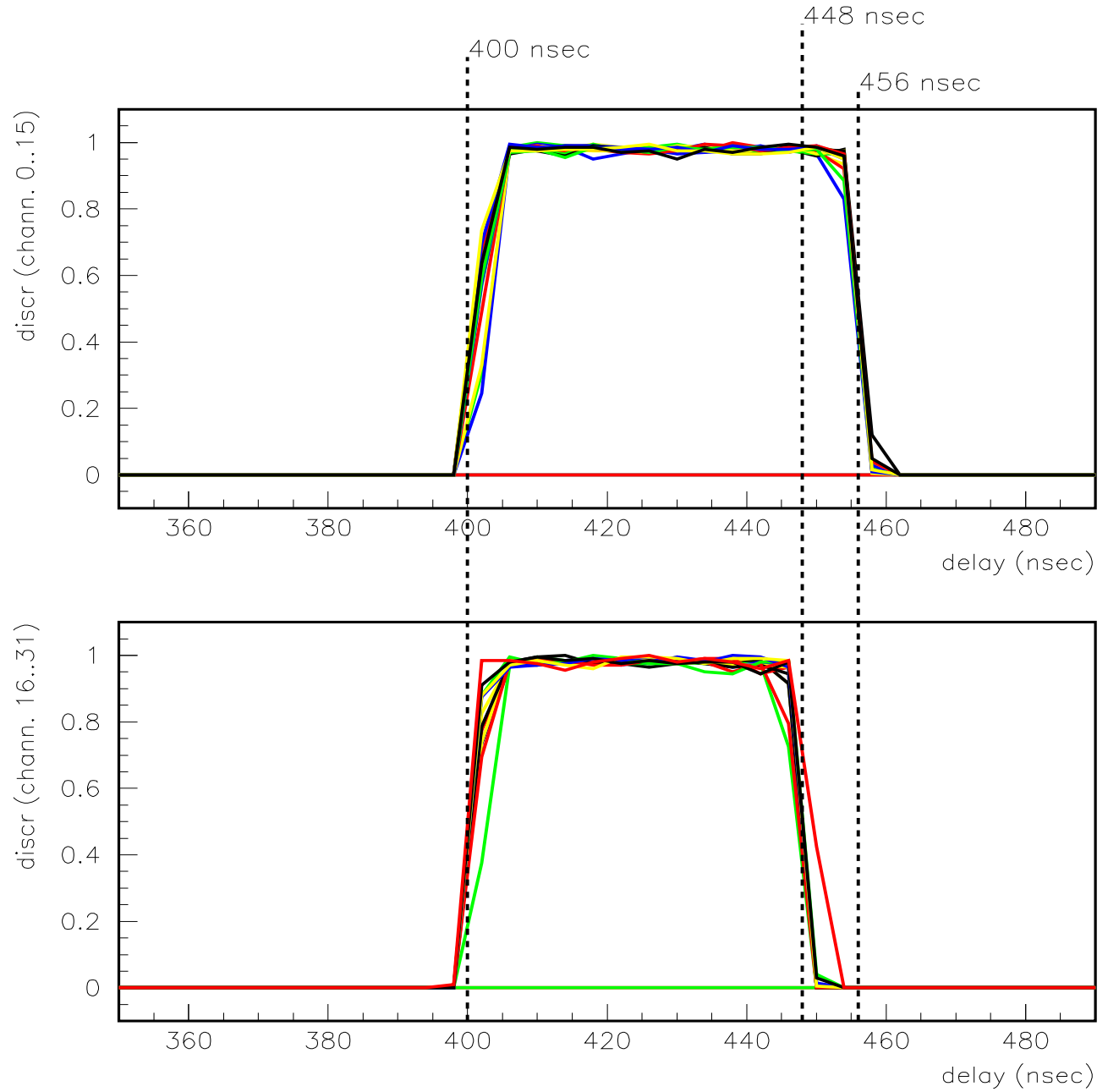
Figure 7: Timing scan for MCMIIc-1-Trip2.

2.1   Results of the Charge Injections Scans.

From the discriminator turn-on curves presented in Figs. 1, 2, 3, 4, 5 and 6 we conclude:

- In MCMIIb, there is a layout problem that causes several low numbered channels in TriP 1 to turn on for larger input charge than most of its neighbors. The problem is caused by too close physical proximity of the discriminator output lines to the input lines.

- MCMIIc has one channel (Ch31) that turns on earlier than expected (50% occupancy around 5 fC). Careful inspection of the data also shows a systematic shift in the threshold for Ch27, 28, 29 and 30. This shift is systematically repeated in the two instances of MCMIIc (-1 and -2) we have tested. It appears there is a layout issue very similar to what was observed on MCMIIb Trip-1, but less dramatic. It appears to be a layout problem similar to the case for Trip 1 on MCMIIb. For MCMIIc-1, there are also 2 channels where the discriminator never fires, this is due to a problem in an electrical contact between the TriP chip and the FPGA in MCMIIc-1, the problem was caused by the repeated probing of the trace that was needed in the debugging stages of MCMIIc-1.

- Except for the 2 problems described above, that are most likely features of the layout and can be corrected in a future version of MCMII, the seven chips studied here present a total spread in the the discriminators of 4 fC or smaller. This is within the design specification for the TriP chip. (This total spread is measured along the 50% occupancy line.).

- We observed a 48 nsec window where the discriminator fires for a 20 fC charge injection. This window is acceptable for the operation of the TriP chip.
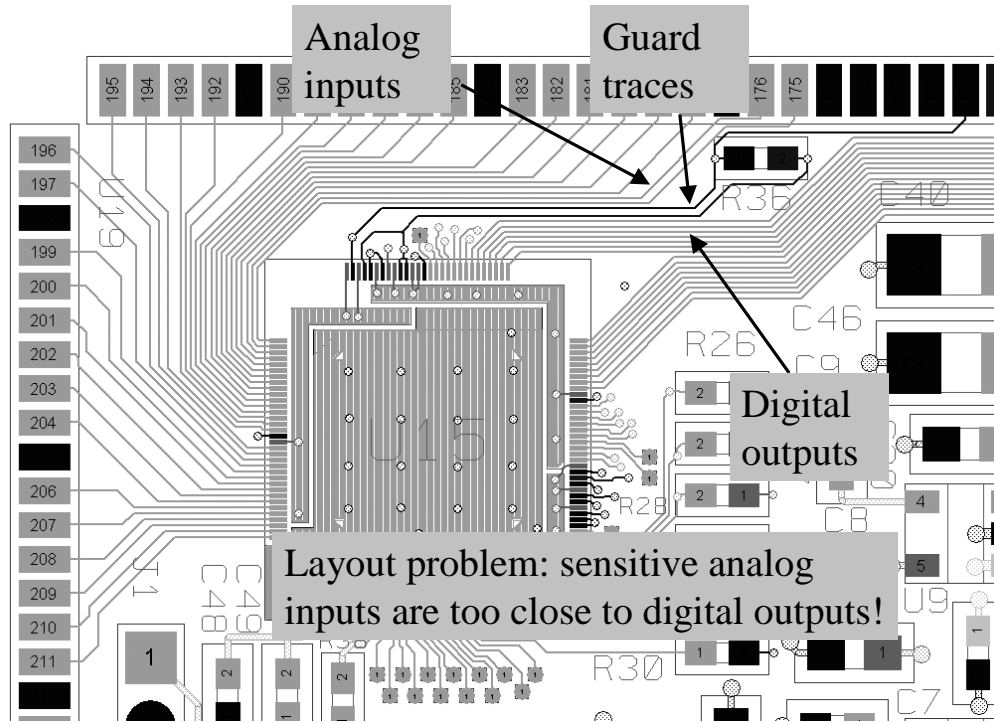
Figure 8: A detail of the layout of the MCMIIb for TriP 1 showing how the discriminator output lines are too close to the analog inputs. The input lines correspond to Ch0 through 8.
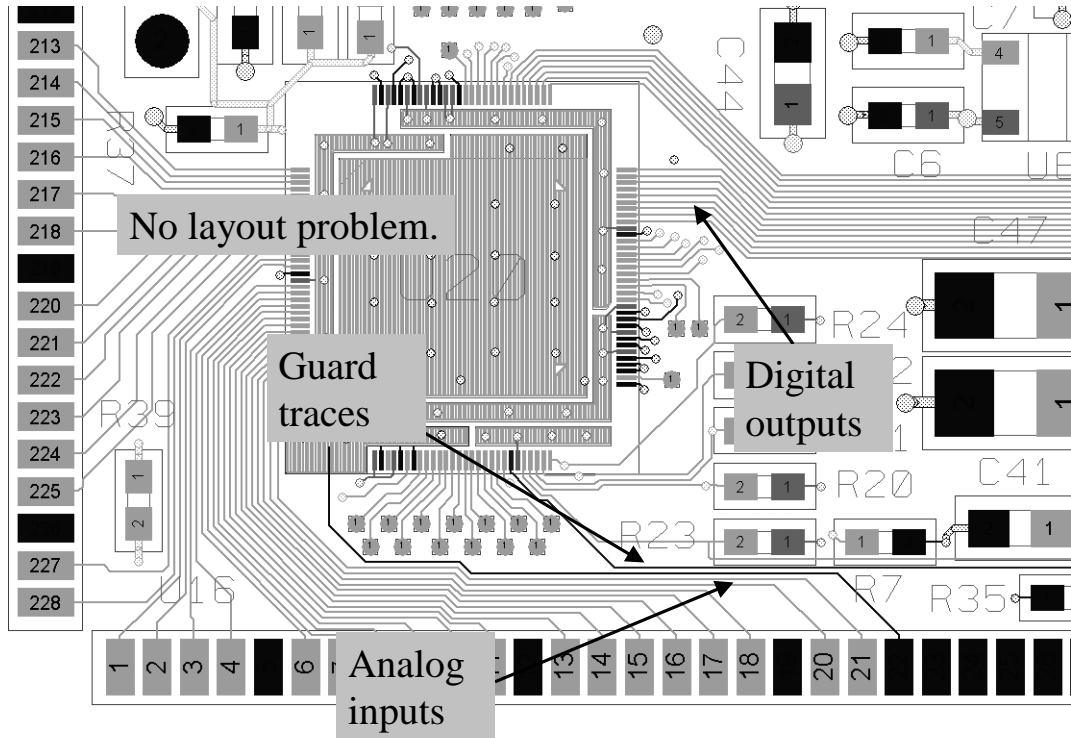
Figure 9: A detail of the layout of the MCMIIb for TriP 2 showing how the discriminator output lines are not close to the analog inputs. Here there are no problems as seen in TriP 1.

3 Analog Readout

In MCMII the analog output of the TriP chip is presented to a commercial ADC (AD9201), there is one AD9201 for each TriP. The digital output of this ADC is read by the FPGA (also mounted on the MCM) and combined with the discriminator information before it is sent to the Stand Alone Sequencer (SASeq) for readout. In this section we do some tests of this aspect of the system. The ADC has 10 bits, for these tests we have discarded the two least significant bits.

The signals required for the analog readout of the TriP chip are described in Ref. [1]. A scope picture of these signals is shown in Figs. 10.

The analog output of the TriP chip can also be studied as a function of the ammount of injected charge, the results are shown in Figs. 11 and 14, for MCMIIb-1 using Option (A) of Table 2 with 33 pF capacitor at the input (the effect of the 33 pF will be discussed later on this note). A linear fit was done for each channel to obtain the pedestal position and gain (ADC counts per fC injected). The parameters for the corresponding fits are shown in Figs. 12 and 15.

Another interesting aspect of the TriP that we need to consider is the variation of gain and pedestal as a function of channel position. For this reason, we look at the parameters for the fits in Figs. 11 and 14 as a function of channel number, the results are shown are shown in Figs. 13 and 16. Again we see that the pedestal spread is dominated by the layout issues for TriP 1. It should be noted that this chip was not operated in a way that minimizes pedestal spread- this is simply because, at this level, the pedestal spread is not an issue.
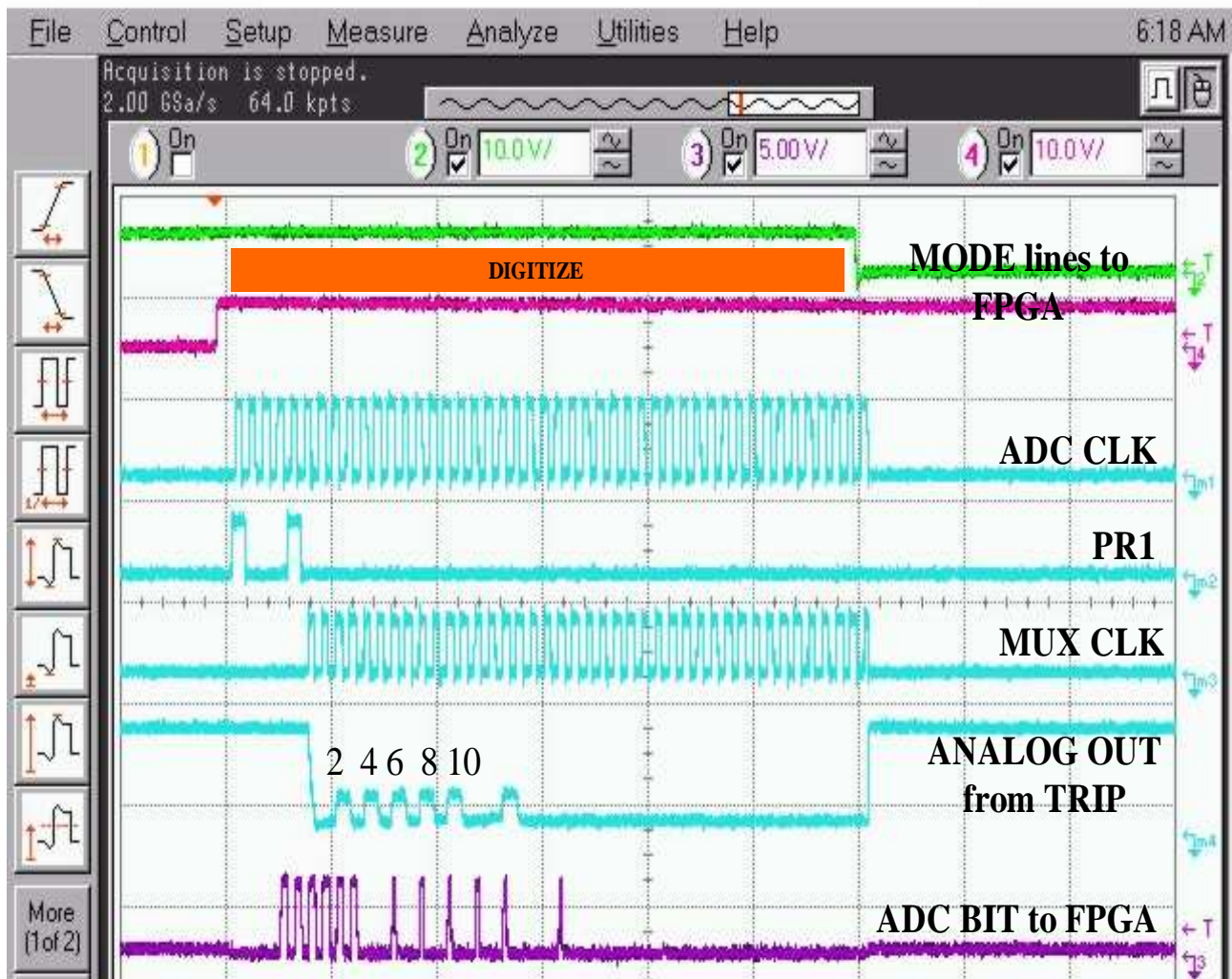
Figure 10: The two top signals in this picture are set by the SASeq and determine the mode for the MCM (green=Mode 0, purple= Mode 1). The system is in ACQUIRE mode until the purple MODE1 raises and starts the DIGITIZE mode, in which the analog output if presented to the AD9201, digitized and read by the FPGA. The ADC clock (3rd signal from the top) starts running in DIGITIZE mode, and the MUXCLK signal starts the analog output of the TriP. One can also see in the picture the ADC output as seen by the FPGA after the digitization was done.
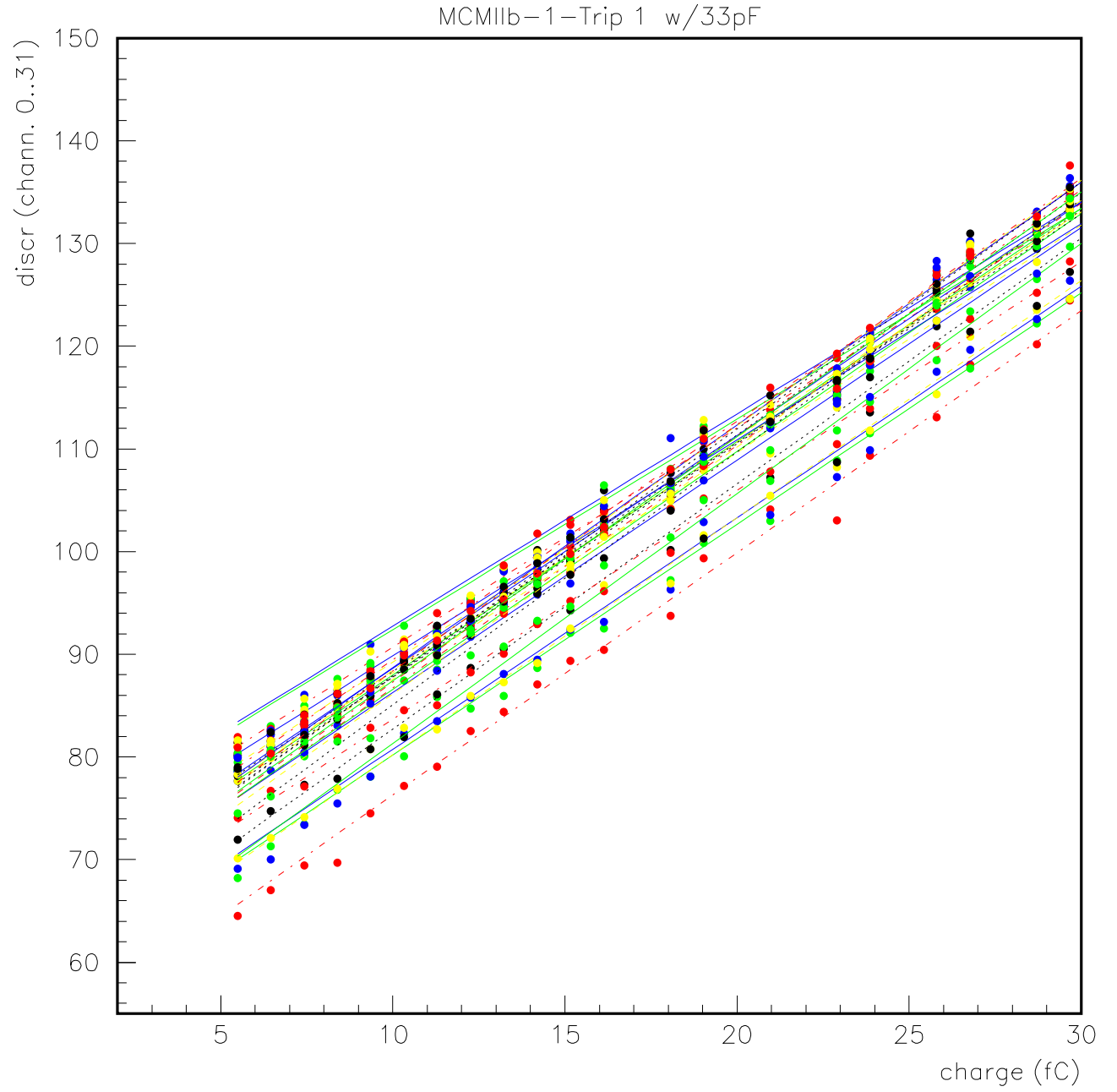
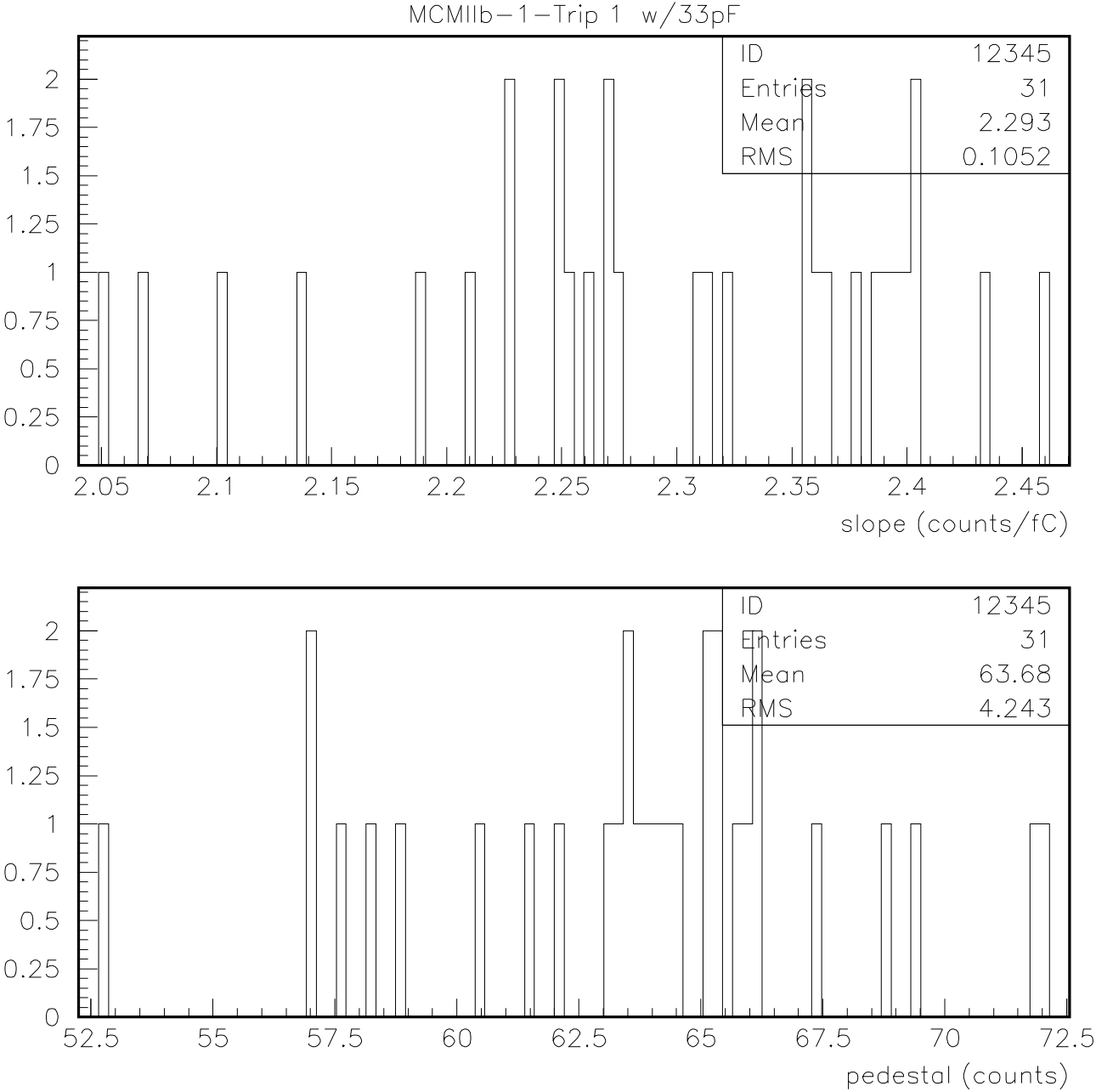Figure 11: Analog output for charge injection scan in MCMIIb-1-Trip1.

Figure 12: Top: Gain for individual channels in MCMIIb-1-Trip1. Bottom: Pedestal for individual channels in MCMIIb-1-trip1. Note the zero is suppressed. The gain variation is below 5% RMS.
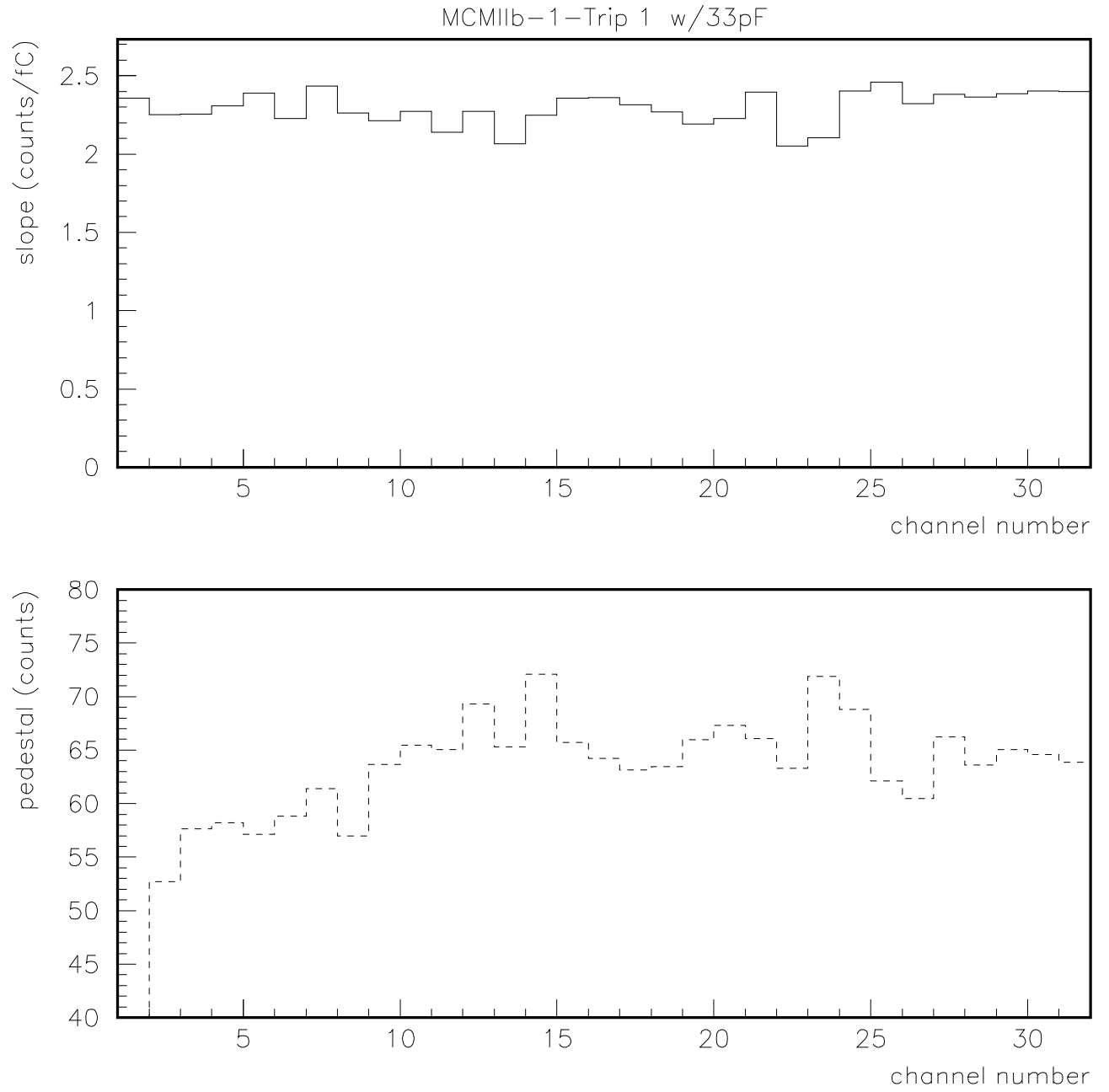
MCMIIb−1−Trip 1 w/33pF

Figure 13: Gain and pedestal position as a function of channel number for MCMIIb-1-Trip1. The effect of layout can be clearly seen for the low numbered channels.
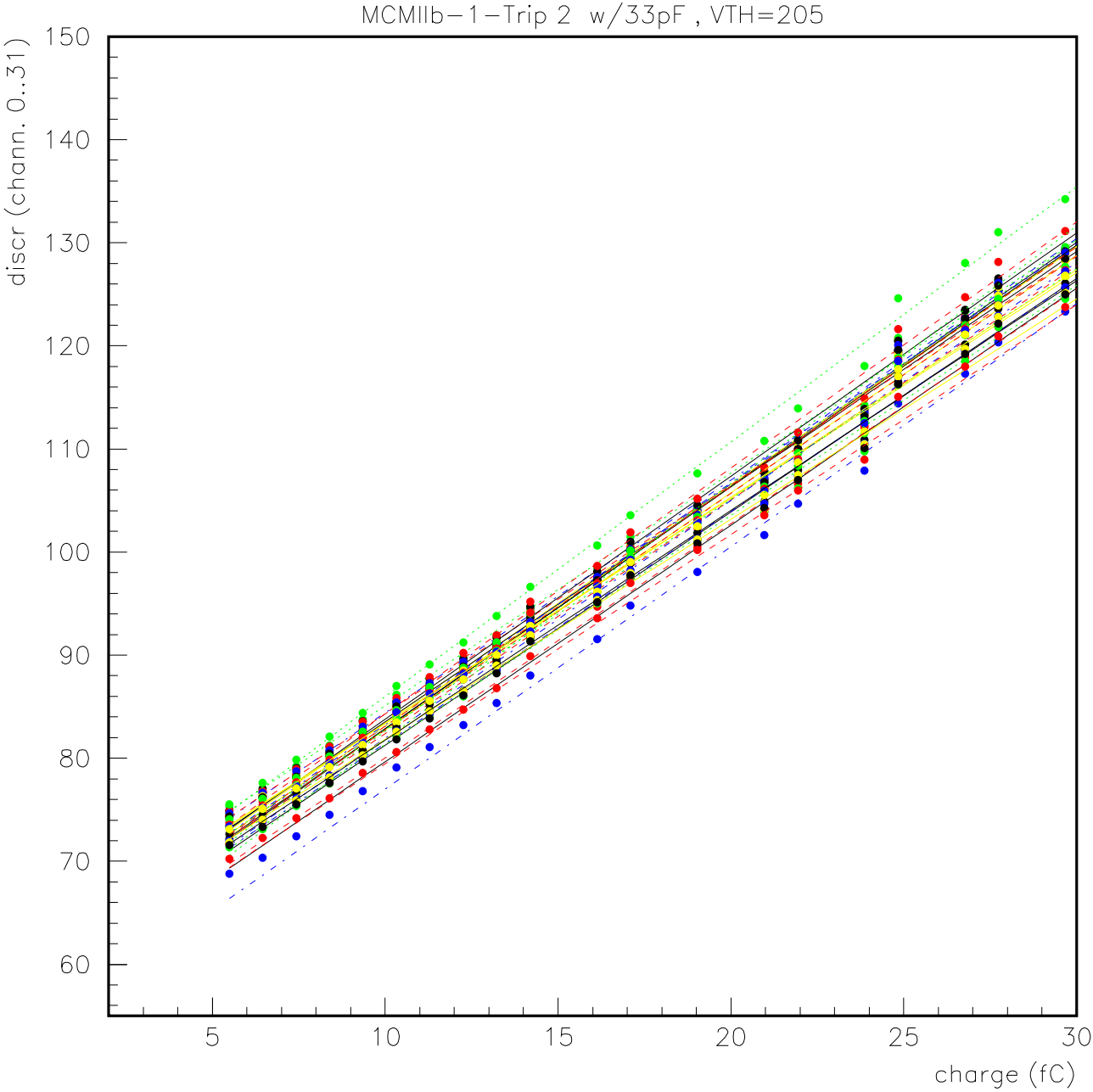
Figure 14: Analog output for charge injection scan in MCMIIb-1-Trip2
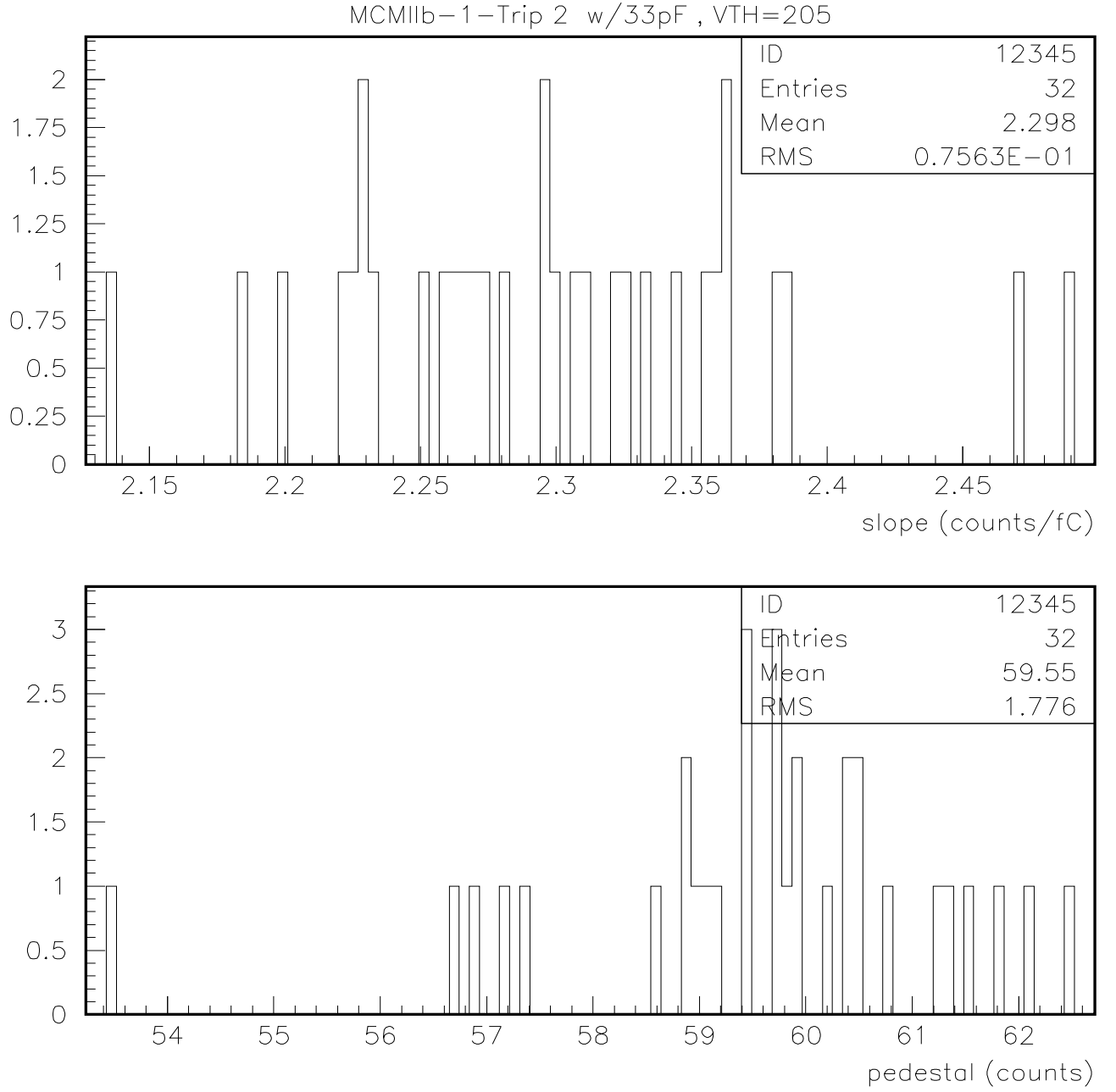
Figure 15: Top: Gain for individual channels in MCMIIb-1-Trip2. Bottom: Pedestal for individual channels in MCMIIb-1-trip2. Note the zero is suppressed
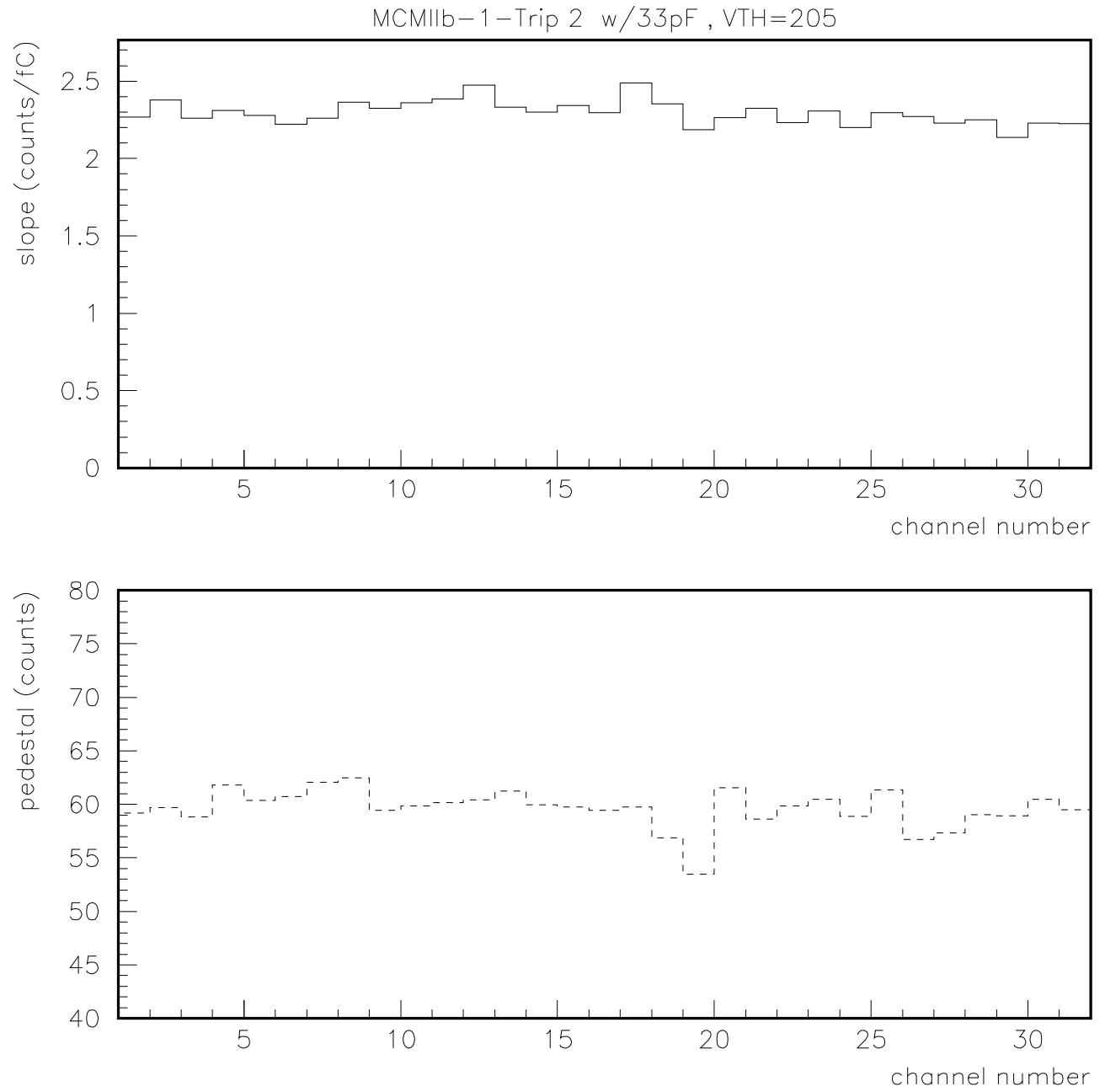
Figure 16: Gain and pedestal position as a function of channel number for MCMIIb-1-Trip2.

3.1 Results of the Analog Readout

- The analog readout functionality of MCMIIb and MCMIIc have been tested successfully. We observe a signal of 100 mV in the analog output for an input charge of 10 fC (this data is taken at the higest gain settings).

- MCMIIb-1-Trip1 has a significant spread in the analog pedestals. The structure of this pedestal spread points to an issue in the layout of MCMIIb for Trip1. Trip2 does not show this large spread in the analog pedestal.

- The calibration parameters in Figs. 11 and 15, show a good linearity response of the ADC and gives a gain of 2.3 counts/fC (with variations of 0.1 counts), that is the same for both chips.

4 Effect of 33 pF Coupling to Ground.

All the discriminator tests described in the previous section have been based on TriP chips with nothing connected to their inputs. In the real application, we expect between 30 and 40 pF of stray coupling to ground (in large part due to the 25pF flex circuit). For this reason, the final characterization of the operation of the TriP chip will be done connecting the input to VLPC channels at DØ.

In our test stand we simulate the conditions at the detector by connecting 33 pF capacitors in the input of the AFE, where the MCM with the TriPs is mounted, and connect the other end of this capacitors to ground.

The charge injection scans were repeated for MCMIIb-1-Trip2 with this new configuration and Option (A), The results are presented in Fig. 17 and a comparison is done for the same TriP without the 33 pF coupling to ground, using different threshold settings for the two cases.

We also perfomed charge injection scans for MCMIIb-1-Trip2 with the 33pF capacitors changing for discriminator threshold VTH=205 and VTH=200, the corresponding curves are shown in Figs. 20 and 18. For each channel a fit was performed using the error function and the corresponding parameters are shown in Figs. 19 and 21. This study also gives a calibration for the VTH setting, the result is $\frac{4.9}{5}$ fC/count = 0.98 fC/count.

From Figs. 18 and 20 one can see that there is approximately a 2 fC shift between the curves for the lower bank (black circles) and those for the upper bank (red triangles) channels in the TriP. We noticed that by inverting the DIGENU signal in the TriP this shift dissapears (see Table 2). A new charge injection scan was performed after inverting DIGENU with VTH=203, and the results are shown in Fig. 22 with the corresponding fit parameters in Fig. 23.

We also performed a delay scan with this new configuration and Option (A) and the results are shown in Fig. 24.

4.1   Results of the of 33pF Coupling to Ground.

- The spread in the discriminators turn on curve is still within the acceptable limits when the 33pF coupling is present and the TriP is operated in Option (A), the spread in this case in less than 5fC, taken as the maximun spread of 31 channels.

- The analog pedestal spread is acceptable with the 33 pF coupling using, from the analog readout studies in Section 3.

- More than 75% of the charge is collected for an integration window of around 40nsec. For 50% of the carge, the window is closer to 50ns.
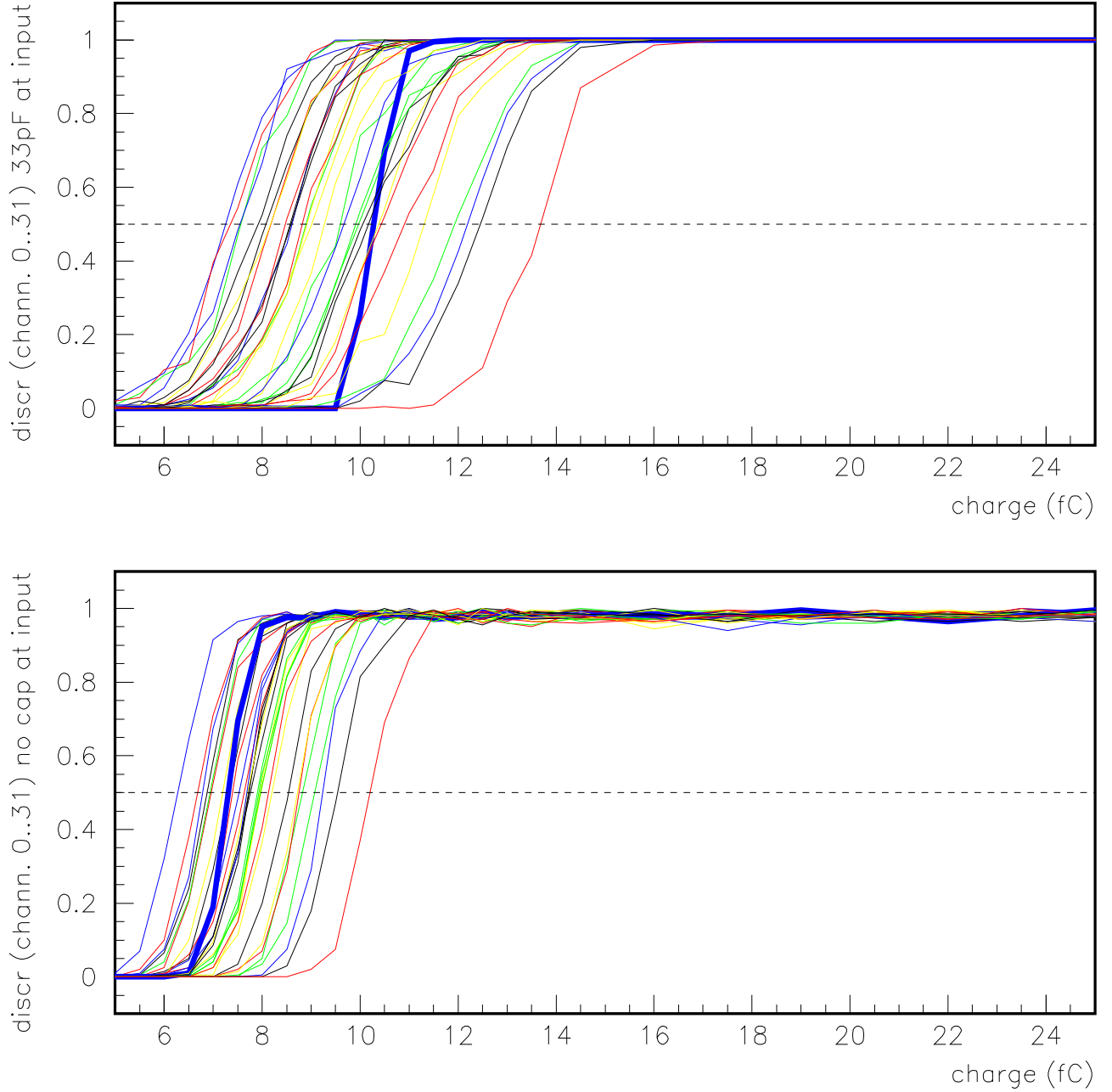
Figure 17: Comparison of the discriminators turn on curve for MCMIIb-1-trip2, with the coupling capacitors using VTH=207 (33fC) and without them using VTH=210.

Figure 18: Discriminator turn on curves for MCMIIb-1-trip2 with VTH=205. The lines correspond to fits using the error function. These are not the best results achieved.

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MCMIIb−1−Trip 2 w/33pF VTH=205

ID	300
Entries	32
Mean	11.66
RMS	1.734

threshold (fC)

ID	400
Entries	32
Mean	1.453
RMS	0.3274

sigma (fC)

Figure 19: Parameres from the fits in Fig. 18.
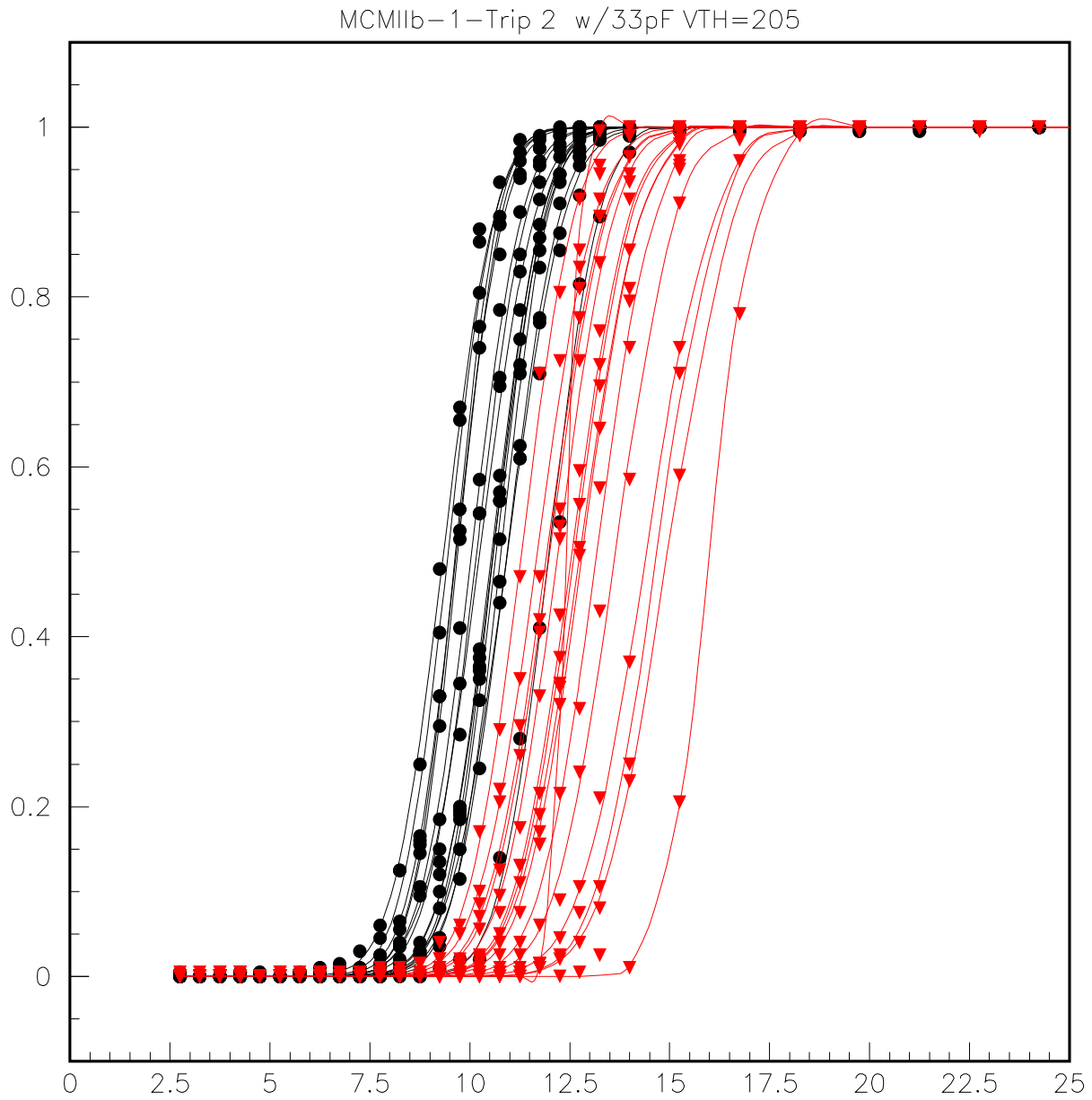
Figure 20: Discriminator turn on curves for MCMIIb-1-trip2 with VTH=200. The lines correspond to fits using the error function. These are not the best results achieved.
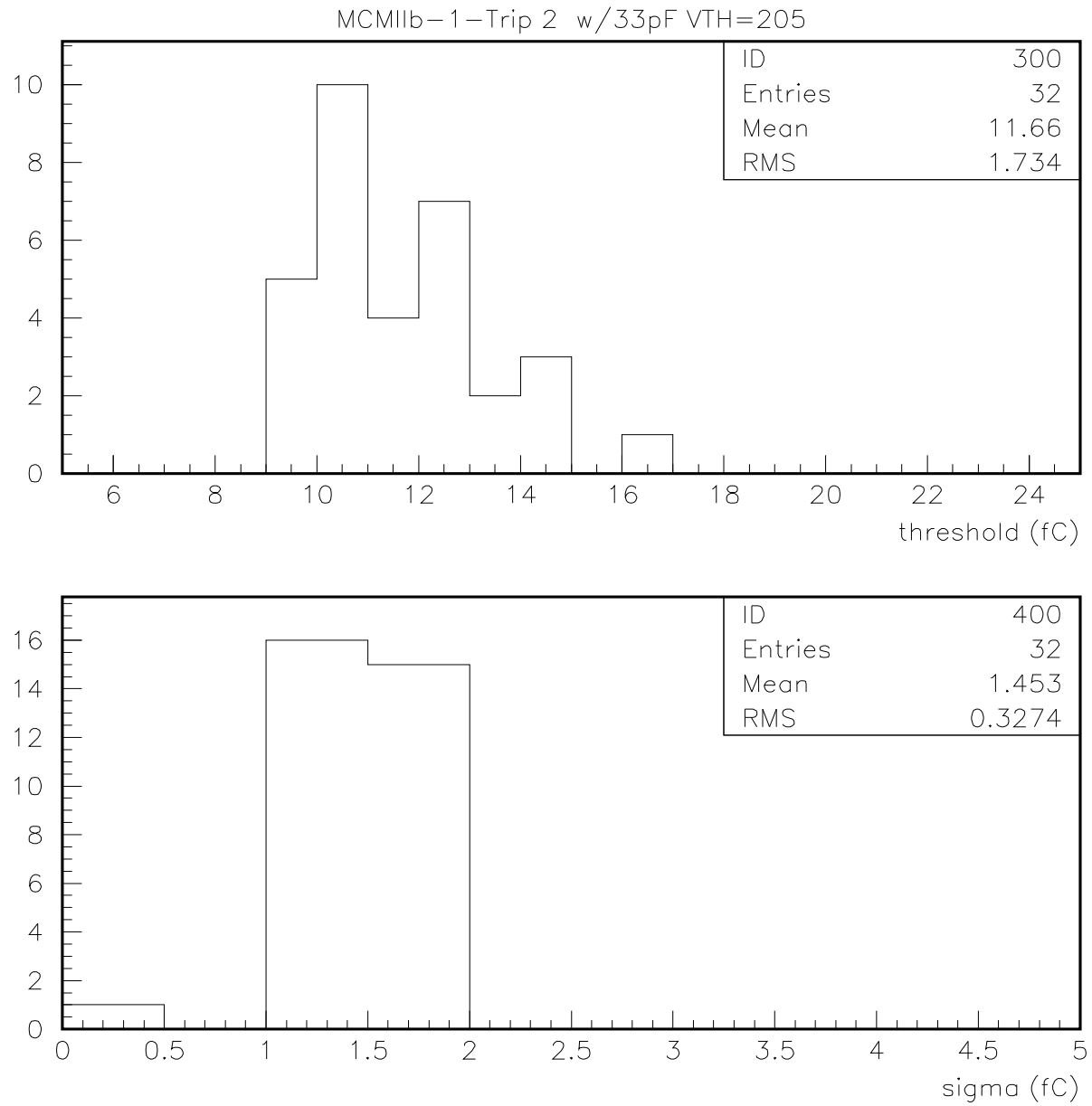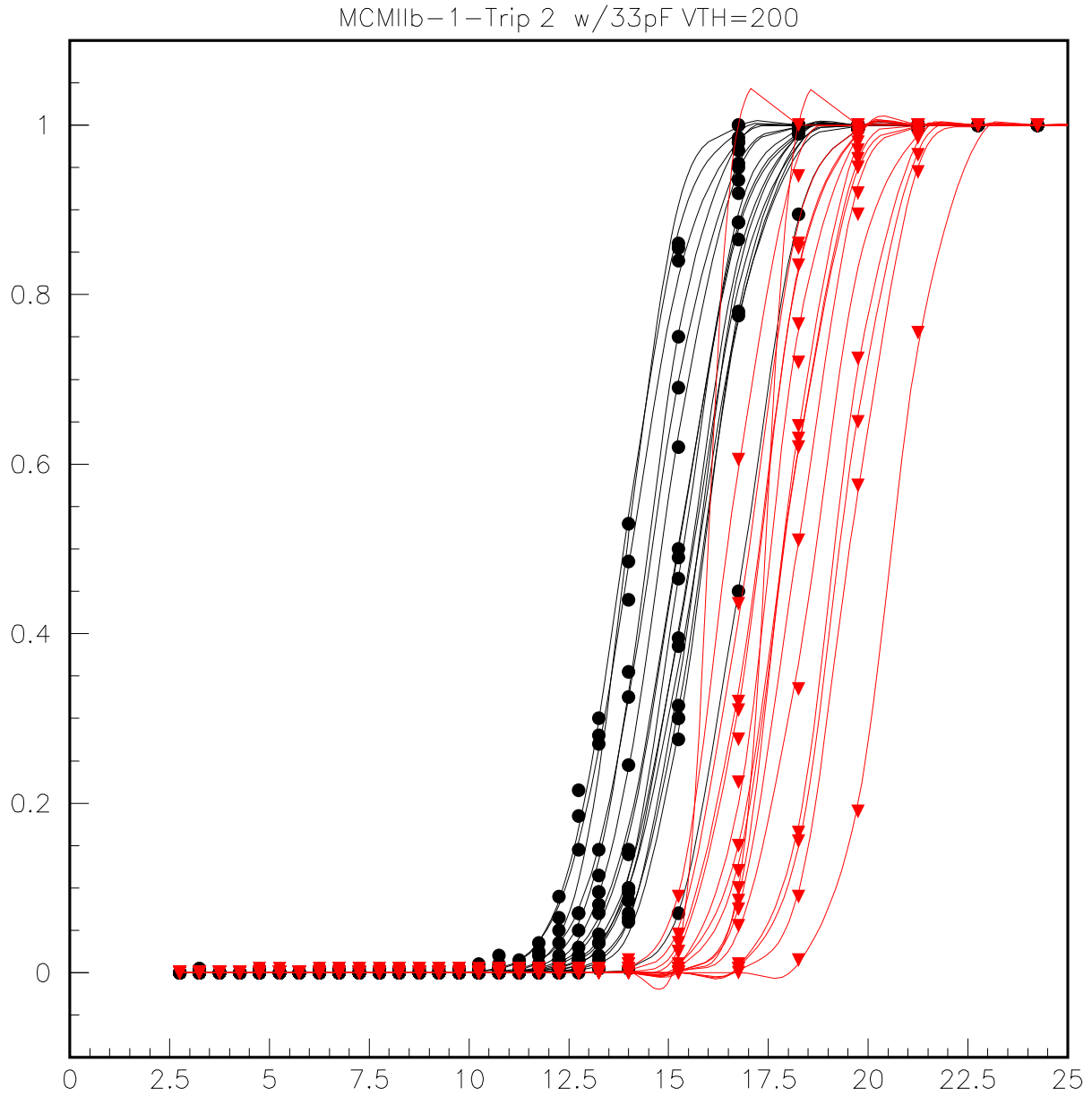
2002/12/23 17.52

MCMIIb−1−Trip 2 w/33pF VTH=200

ID	300
Entries	32
Mean	16.50
RMS	1.785

threshold (fC)

ID	400
Entries	32
Mean	1.484
RMS	0.3950

sigma (fC)
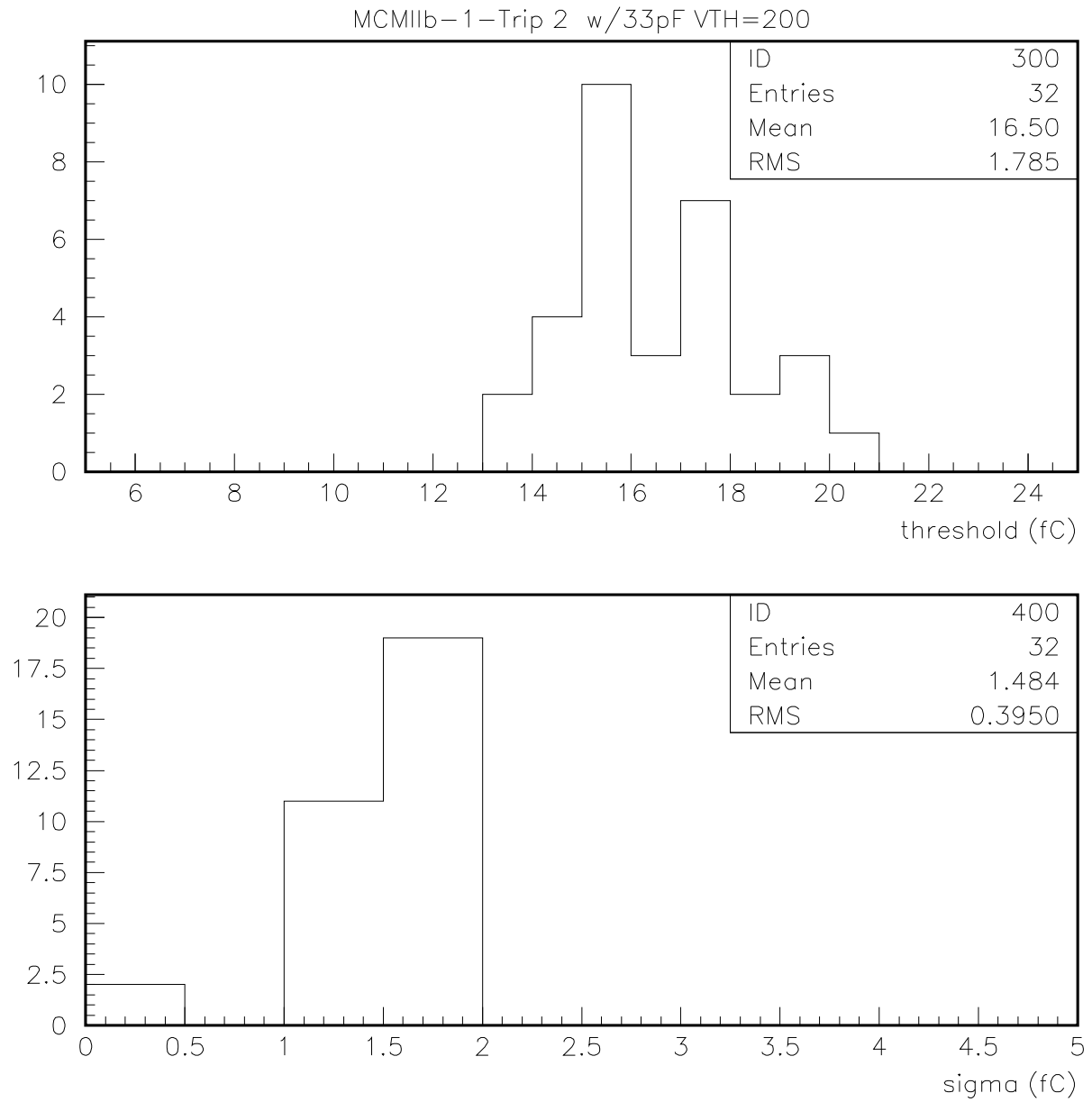
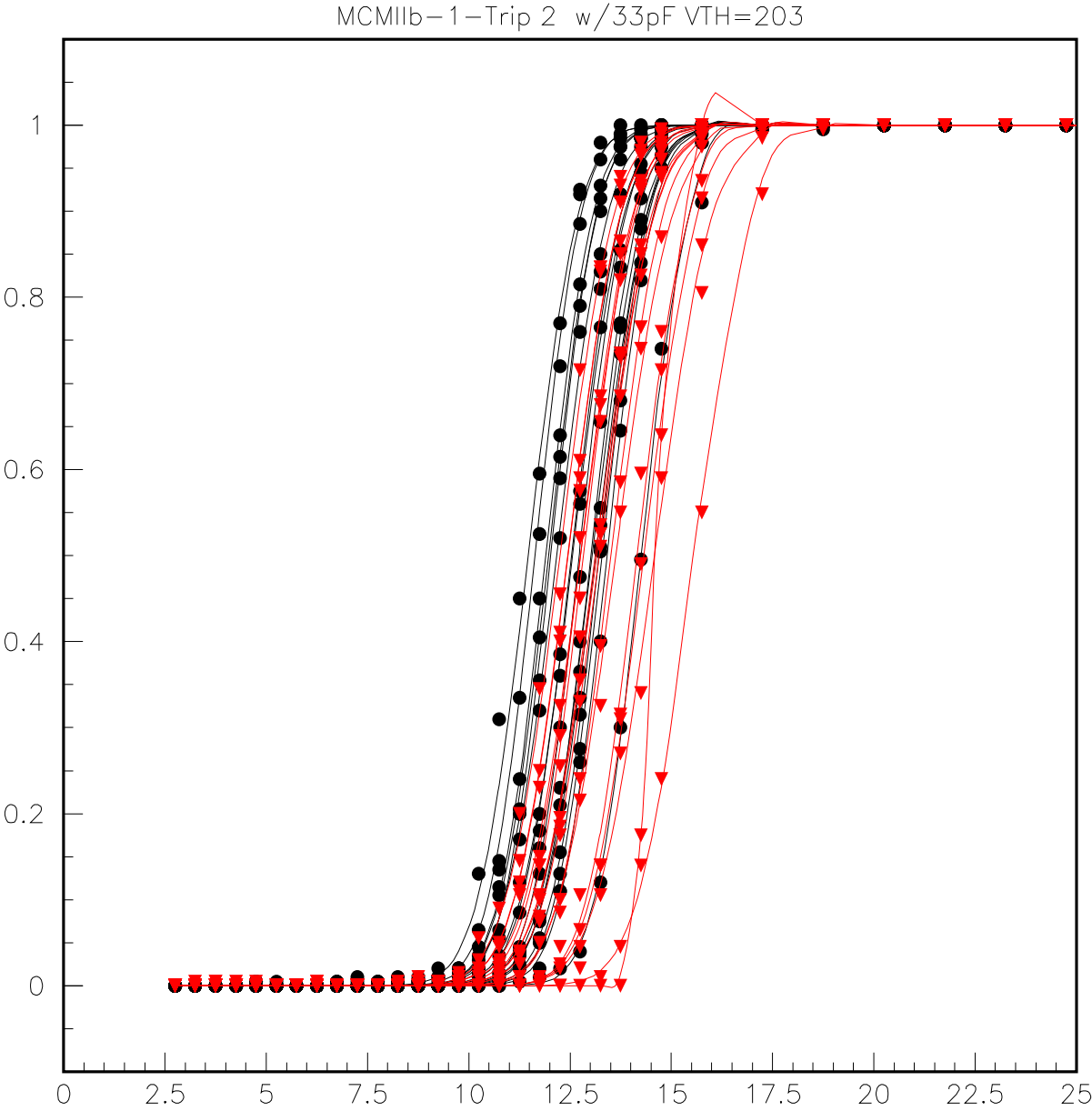Figure 21: Parameres from the fits in Fig. 20.

Figure 22: Discriminator turn on curve with DIGENU inverted. The lines correpond to fits using the error function. These are the best results we were able to achieve.
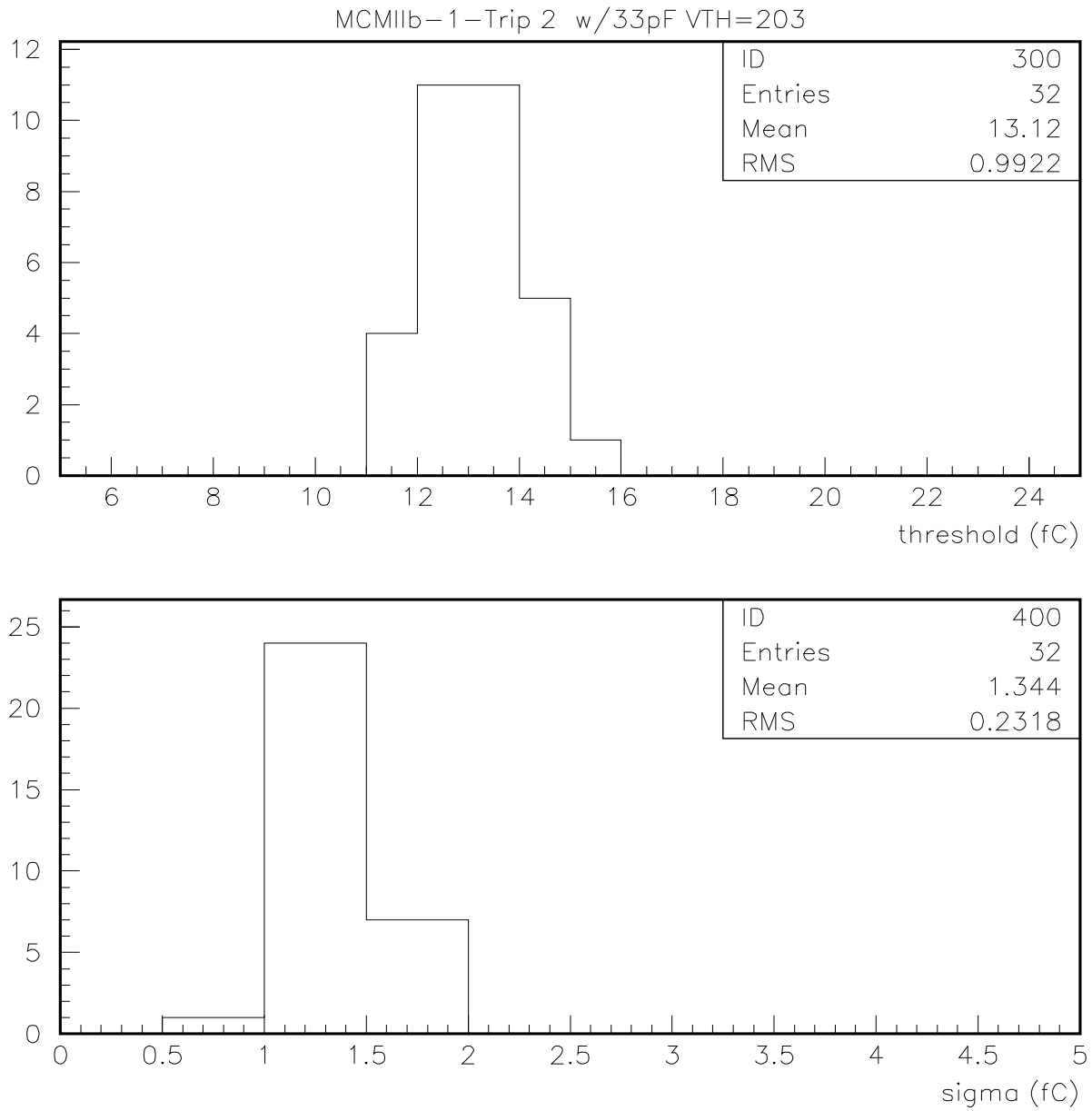
2002/12/23 21.30

Figure 23: Parameres from the fits in Fig. 22.
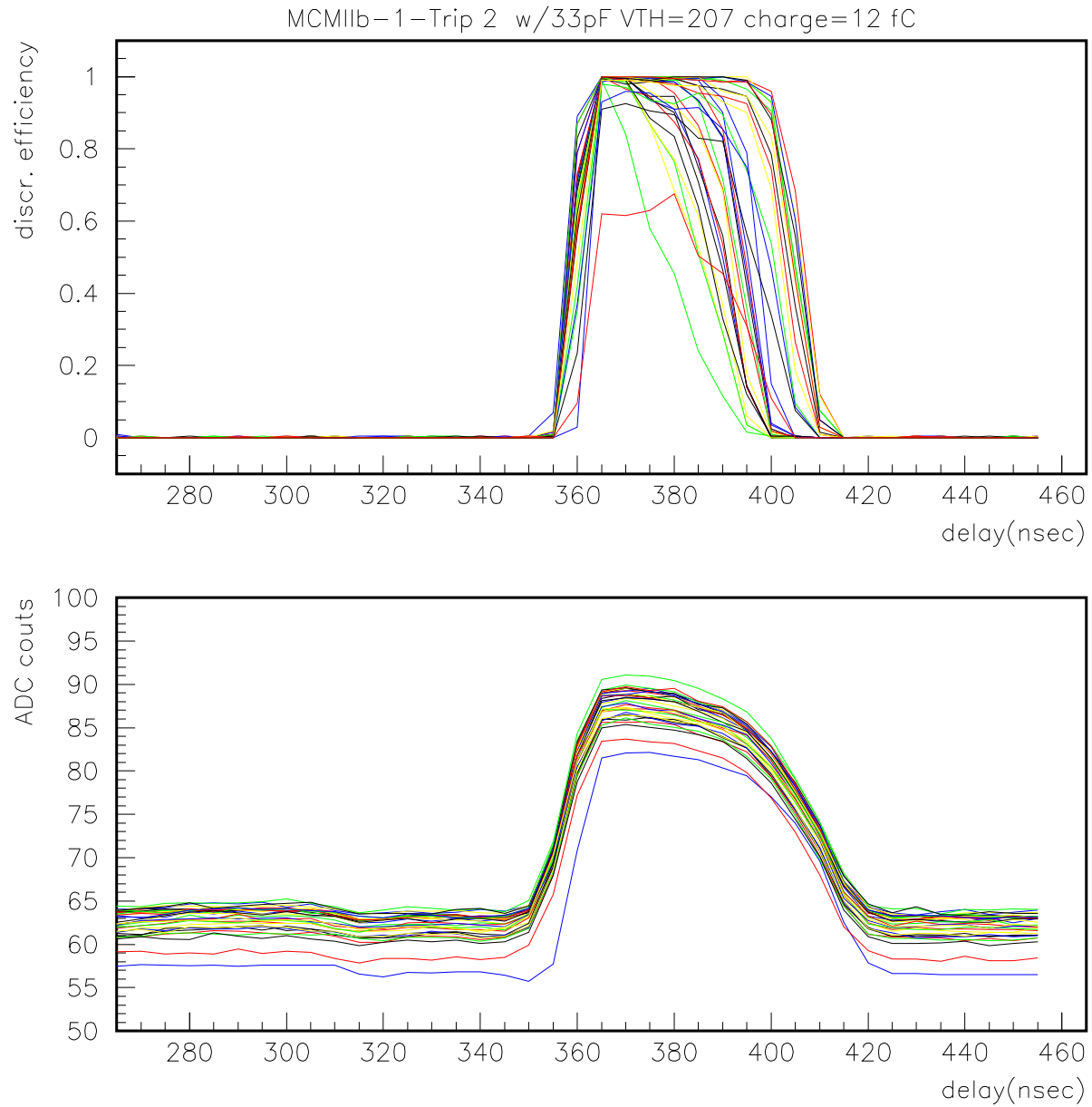
2002/12/23 21.30

Figure 24: Timing scan for MCMIIb-1-Trip2 with 33pF coupling to ground and charge injection of 12fC. Top: Discriminator efficiency. Bottom: Analog output.

5   Timing Options for the Operation of the TriP

As mentioned in Section 1, from the previous studies discussed in [1], we have two options for the operation of the TriP chip.

Option (A) has always one discriminator output bank enabled, and it prevents the TriP from having to swing all 16 channels at once, as happens in Option (B) when both banks are disabled at the same time (see Table 2). In order to understand the performance of the discriminators for this two operating options, we performed a discriminator scan on MCMIIb-1-trip2 for Option (B). The results are shown in Figs. 25.

Figure 25 shows that Option (B) deteriorates the performance of the TriP chip beyond the specifications. The spread observed in the discriminators scan is not acceptable.
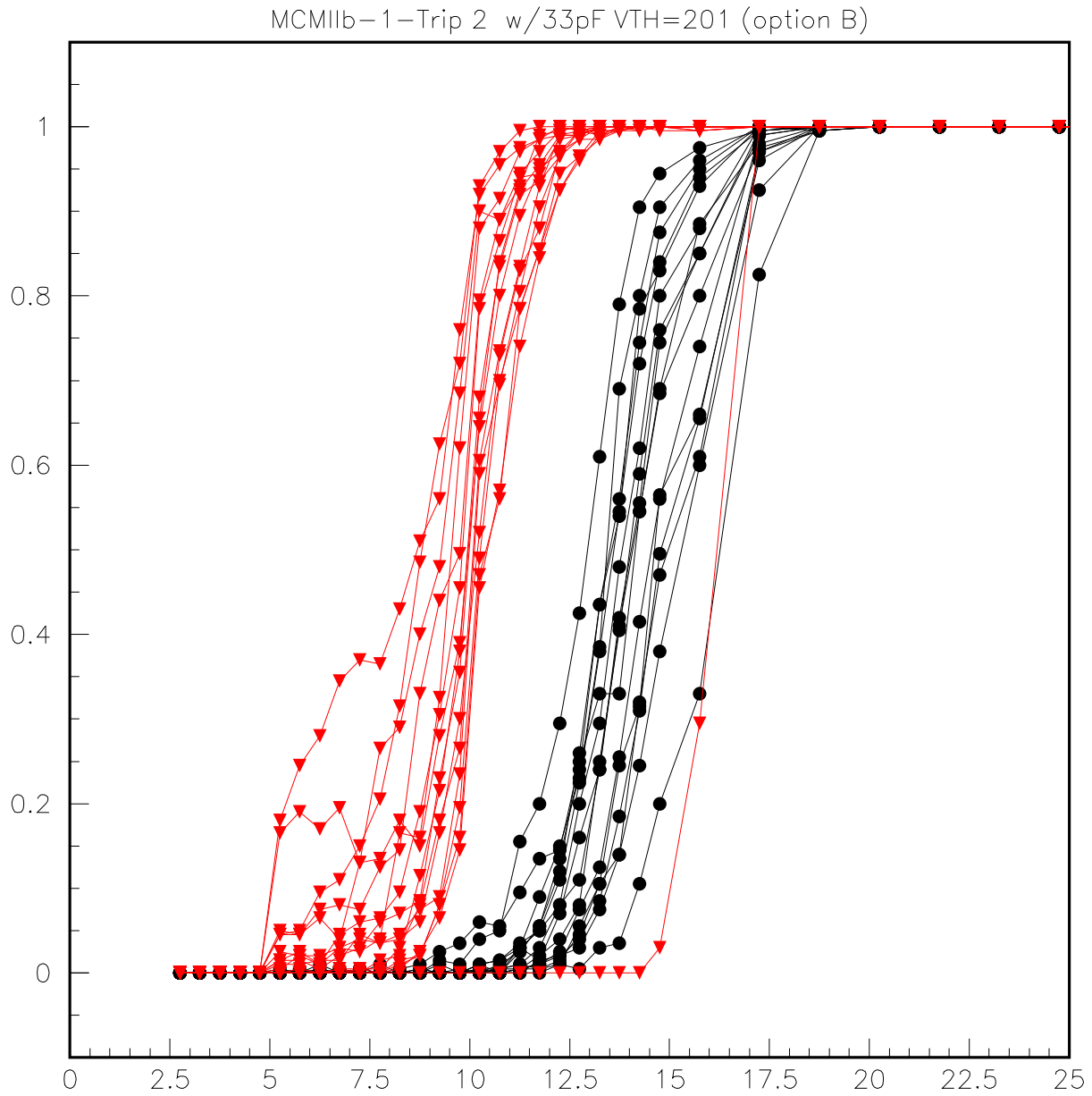
2002/12/23 21.31

MCMIIb−1−Trip 2 w/33pF VTH=201 (option B)

Figure 25: Discriminator scan for MCM1-trip2, for Option (B)

6   Effect of a 25 fC Pulse an Earlier bucket.

All the tests done in earlier sections of this note were done injecting one pulse every 7μsec. In this section we investigate the effect of a pulse in the previous bucket (132ns earlier than the charge injection that we are reading out). The discriminator occupancies as a function of the injected charge in the readout bucket are shown in Fig. 26, with a 25fC pulse in the earlier bucket. It can be seen from this study that the pulse in the earlier bucket moves the discriminator turn-on by approximately 2fC, compared with the discriminator turn-on curves for the same chip with the same settings without the 25fC in the previous bucket shown in Fig. 22. This effect has to be considered as an extra spread in the discriminator curves.
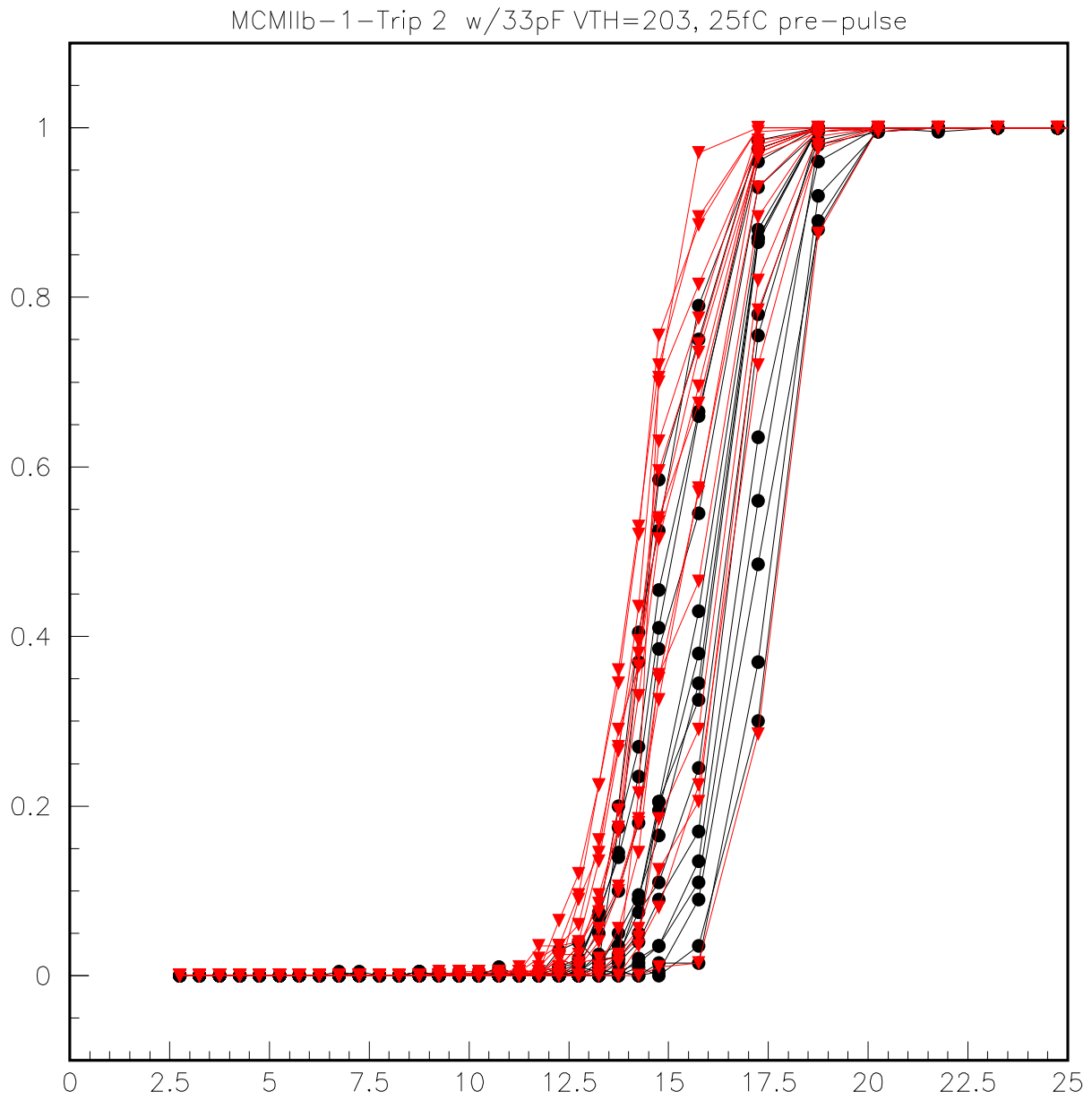
2002/12/23 21.30

MCMIIb−1−Trip 2 w/33pF VTH=203, 25fC pre−pulse

Figure 26: pulse before

7   Test of the Packaged TriP Chip

As mentioned in the introduction to this note, we also tested a packaged version of the TriP chip. The chip was packaged by ASAT in a QFT 100 with an exposed pad that was electrically connected to the back of the die using electrically conductive epoxy. The package was then mounted in MCMIIc-2 and electrically conductive epoxy was also used to connect the exposed pad to the ground plane in the MCMIIc.

The results of the charge injection scan performed on this TriP are presented in Fig. 27. The curve shows that the performance of the packaged part is basically indistinguishable from those of the directly bonded part. This scan was done with VTH=212, intead of VTH=210 (see Table 1). The scan was then repeated with VTH=210 and the results are compared in Fig. 28. We understand that a lot more statistics has to be accumulated before being able to conclude that the package part will work, but the tests done in this section give a positive result.
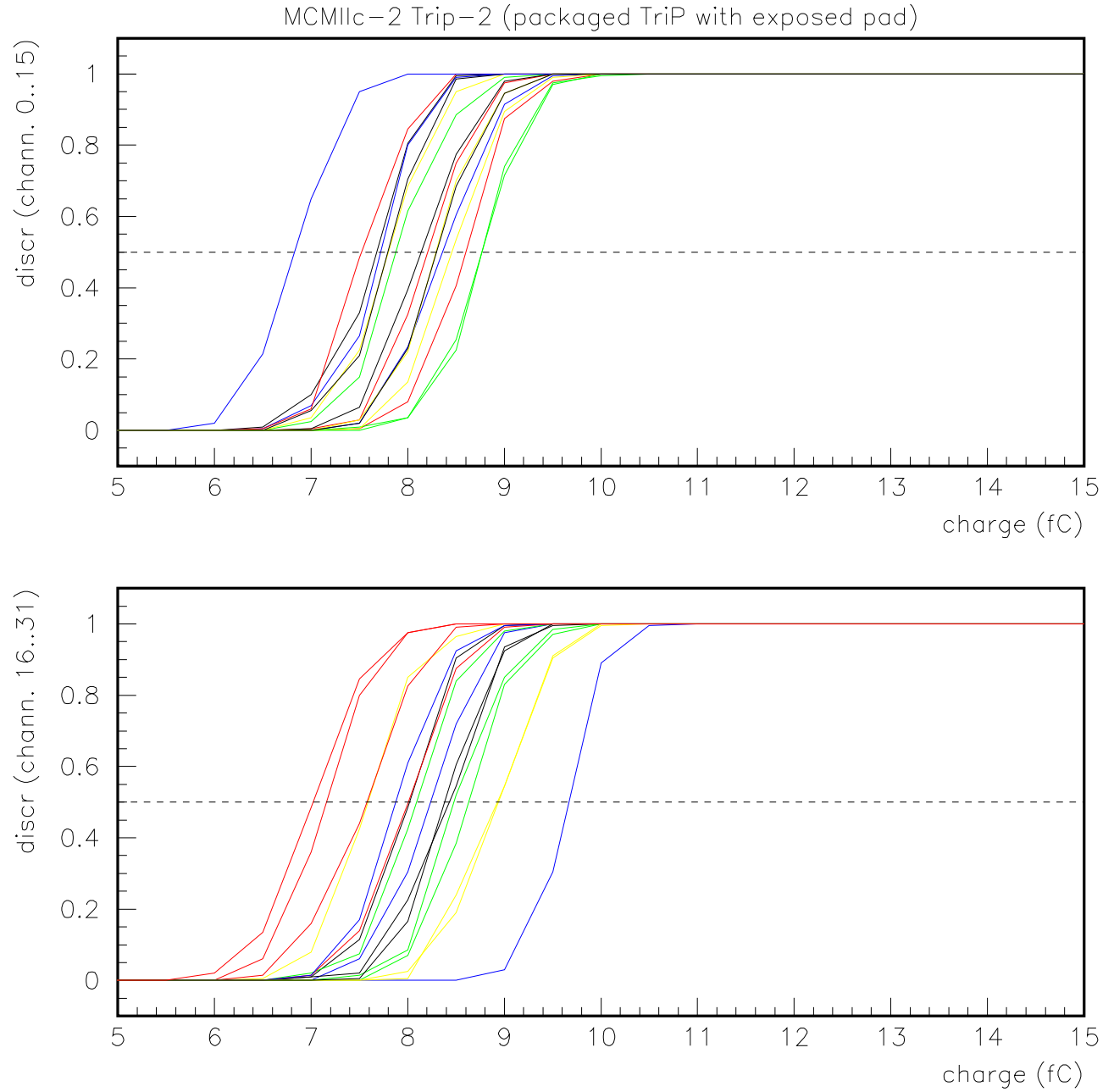
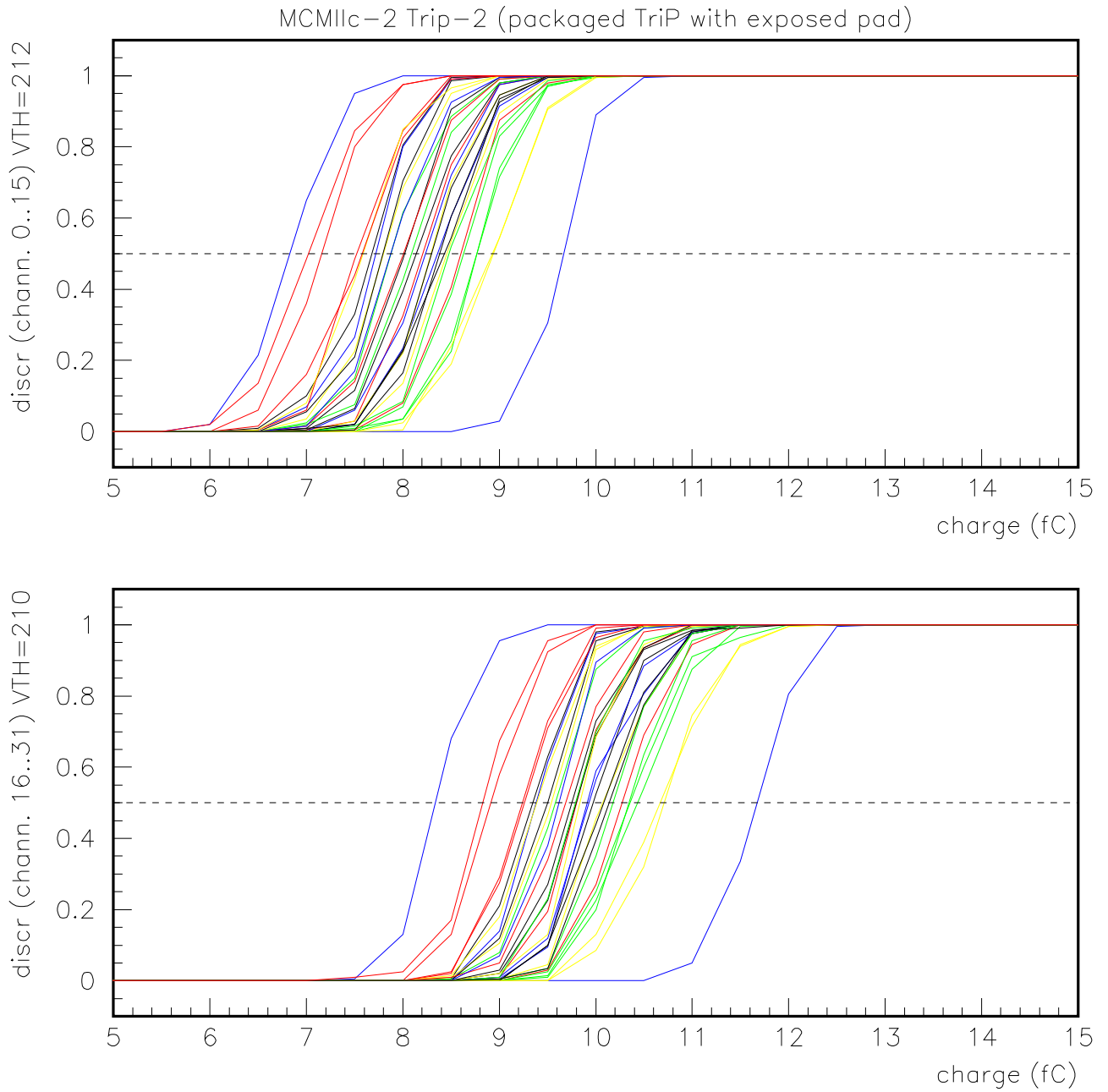Figure 27: Charge injection scan performed for the packaged chip, in MCMIIc-2

Figure 28: Comparison of two charge injections scans for the packaged chip in MCMIIc-2, with VTH=212 (top) and VTH=210 (bottom).

8   Specifications and Conclusions

This section describes how well the TriP chip meets the original requirements as specified in the "TriP Chip Specifications" document [2]. It is also intended to indicate where more testing needs to be done. Also, any discussion of the original specs need to be prefaced with a few important points. First, the specs were not intended to be exhausitve and not meant to be a "minimum acceptable". They were intended to guide the designer in making choices- the goal was always to make something that works on the first try, rather than getting bogged down in a formal specify-design-test-revise cycle with many iterations. Some of the specifications can not be tested easily on the bench, and we expect to continue the test program with VLPCs when a cryostat becomes available.

It is clear from the testing that capacitance on the input significantly degrades the performance. This is not a surprize- any external noise source which couples to the input of the chip is likely low impedence and therefore the charge noise seen at the output of the TriP is directly proportional to the the capacitance at the input. This also means that it is important to test with the actual capacitance seen with the cryostat and VLPC: the 33pF caps we used as the load are a convinient value, but are perhaps a little larger than we expect in the final configuration - the flex cable is about 25fC and the VLPC itself contributes very little. The other stray capacitance on the board and MCM contributes approximately 10fC but it is also there in addition to the 33pF load caps in the bench top configuration. So the total load seen our tests is up to 20% larger than expected in the final configuration.

We also expected that further optimization is possible. The chip has a number of programmable DACs used to set various bias currents. These DACs were set to values that gave good performance of a single chip on a dedicated test board: they has been no effort to optimize these setting for the case of the AFE/MCM. In addition, we know the chip is sensitive to the details of the timing of the control signals and little effort has been spent to optimize the clocks. Overall, we expect that further incremental improvements are possible, but we do not expect any dramatic improvements.

- The number of channels tested makes any conclusions based on this data preliminary.

- The large difference between the performance of the chip with and without caps indicates

that the largest sources of noise are likely outside the chip.

- We see no difference between the performance of the packaged chip vs. chip bonded directly to MCM substrate.

- Allthough some specifications are not met when 33pF capacitive load is added on the inputs, it is likely that the the fiber tracker would function at 132ns even if the results could not be improved by further optimization. However, it is imperative to perform tests in a more realistic configuration (with the cryostat and VLPCs).

- We have tested 10 TriP chips, and 9 of them appear 100% functional (including 8 on MCMs and 2 stand alone). This leads us to expect a very good yield from the 7000 TriP die produced.

- It is known that simple fix (involving negligable risk) to the chip would allow for the DISCR outputs to be made active only during reset. This would result in improved performance and allow additional flexibility in optimization. In particular it would increase the charge collection window by about 10ns and reduce the spread between ch by at least 1fC.

Table 3: This table indicates the main requirements for the TriP as they were given prior to the design of the chip and the corresponding results of the testing (if any). All charge values are input reffered.

Window for charge collection: 50 to 70ns.	40 to 45ns	Not optimized yet. Probably ok.
Digital outputs:		
risetime controlled active only during reset	no no	No, but work around was found.
Threshold setting:(high gain)		
0 to 100fC with 7bit control	satisfied (prelim)	More testing, especially with larger inj charges would be usefull.
99% of channels within 4fC	4fC w/o caps 5fC w/33pF acceptable	Packaged part, no load.
rms noise <1fC	<1fC w/o caps 1.3fC w/ 33pF acceptable	Packaged part, no load. 33pF load.
Threshold setting:(low gain)	not yet tested	
Analog outputs:		
16:1 analog mux at 7.6MHz	satisfied	
ch to ch uniformity within +-3%	6% slope, 3% peds 8% slope, 5% peds satisfied	Packaged part, no load. 33pF load. Some spread is due to layout of MCM.
rms noise <1fC	0.6fC RMS w/o C satisfied 1.2fC RMS w/ 33pF acceptable	Packaged part, no load.

References

[1] "MCM II and the TriP Chip", J. Estrada, C. Garcia, B. Hoeneisen and P. Rubinov, DØ Note 4009.

[2] "TriP Chip Specifications" B. Hoeneisen, rev 12 Dec 2001 by P. Rubinov.